

Nyheter i Version 1.80

Polygon creation

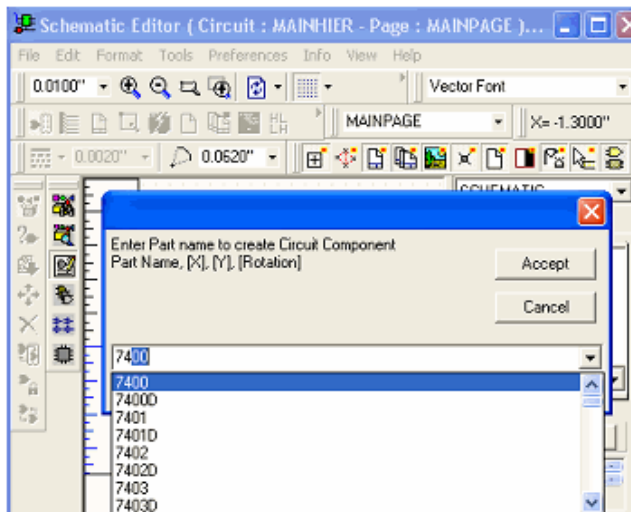
Now polygon creation is implemented in Schematic Editor's Design notes and Notes and Graphics section.

Round Mitered Polygon

Now it's possible to change the pointed vertices of polygon to rounded polygon by inserting arc. This feature is implemented in the Design notes and Notes and Graphics section. For this select the stretch item function tool and select insert round miter option tool. Now clicking on a polygon vertex the radius popup band appears. Choose the appropriate radius; the pointed vertex will get replaced with an arc of specified radius. Also remove miter and remove arc options are available. The remove miter option deletes the arc and the polygon vertex appears as it was before inserting arc. When option remove arc is taken and click on an arc vertex, the arc get replaced with a line linking the end points of arc.

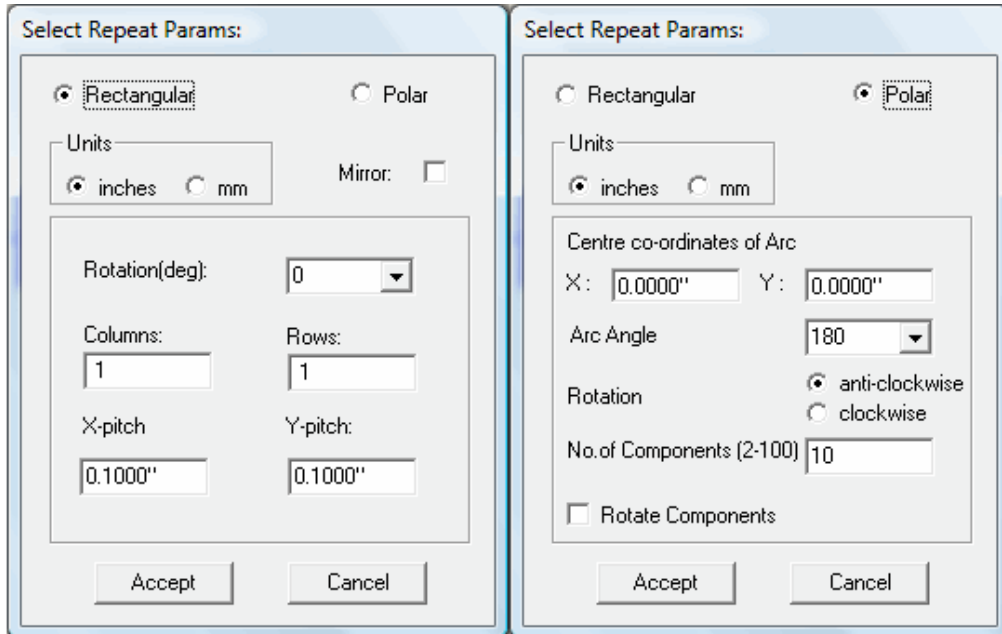
Auto complete of Component names

Auto complete Component Name feature predicts the component name, Package Name or Symbol Name that you want to type in without actually typing it in completely and speeds up your search for a component to add to your design. This option automatically suggests the predefined components when you try add new Symbols in Schematic Editor.



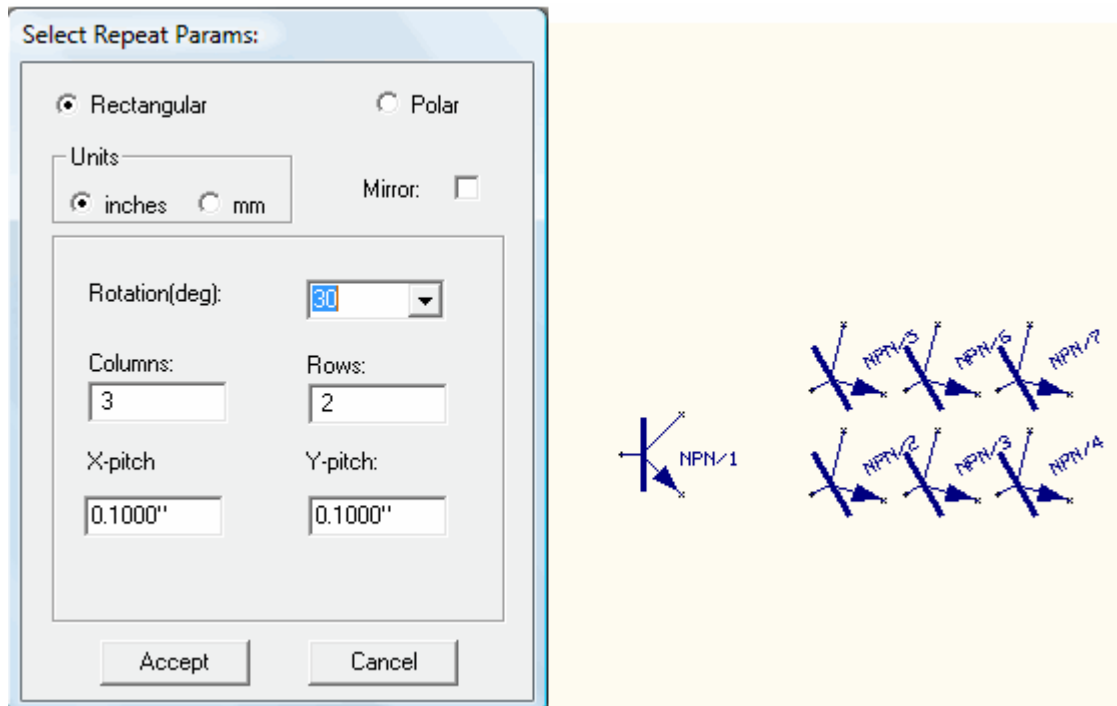
Step Repeat Component in Rectangular form or Polar form

This is a new feature in the Schematic and layout Editors for adding components in Rectangular form or Polar form.

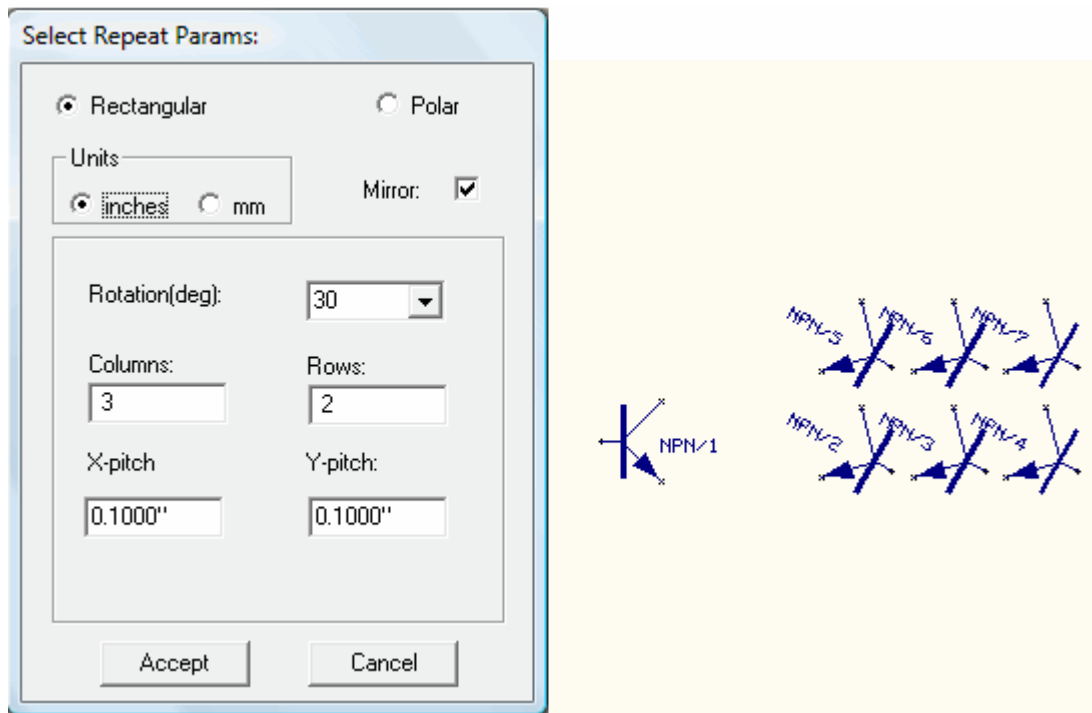


Rectangular Form

In Rectangular Mode, can specify different parameters like component rotation in degrees, No. of Columns, No. of Rows, X-pitch (horizontal distance between the components) and Y-pitch (vertical distance between the components).

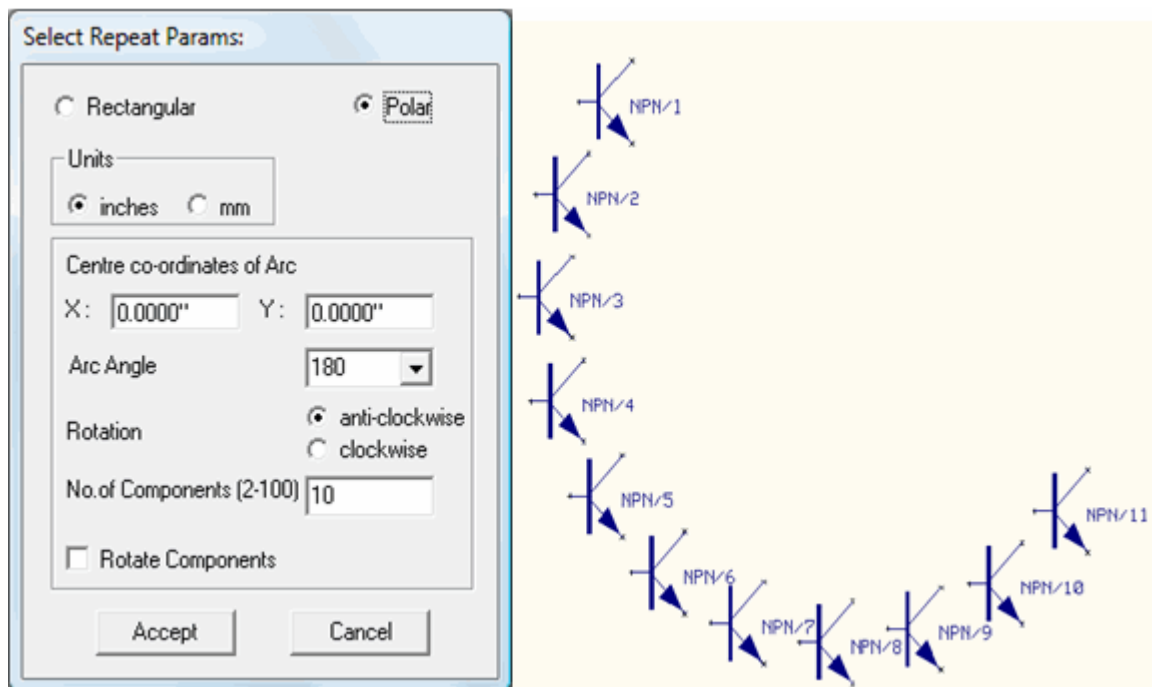


The output with same parameters, with mirror option enabled is given in the figure below.

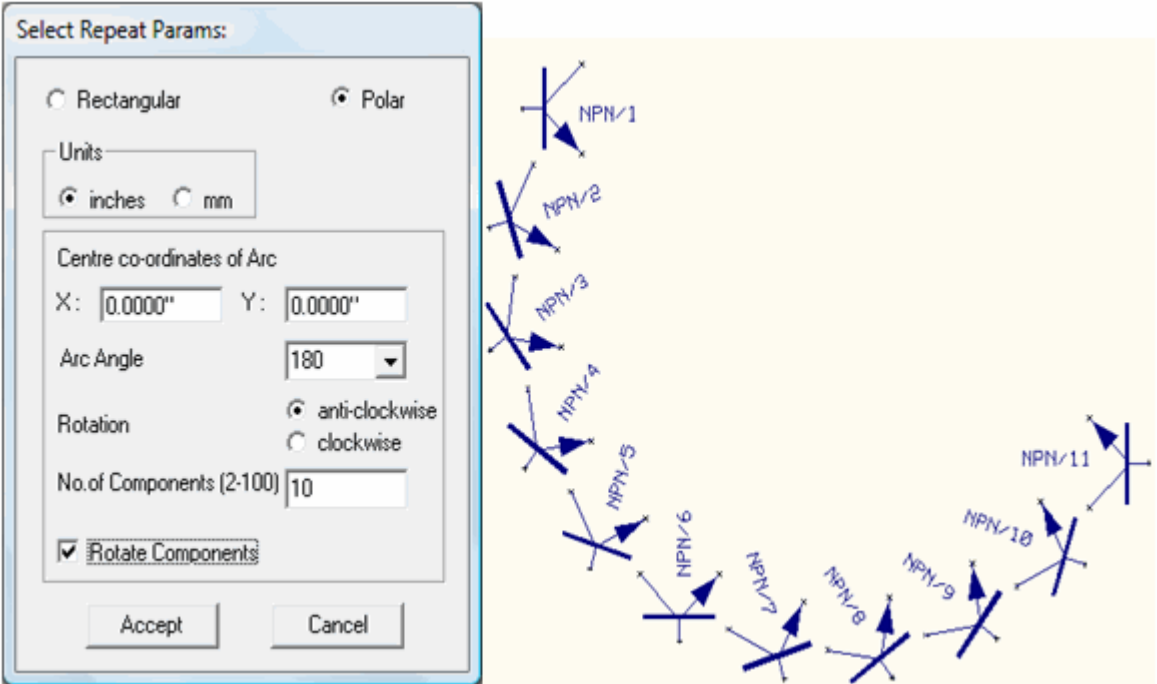


Polar Form

In Polar Mode, can specify the required arc angle and the no. of components to be placed in that arc angle. For repeating components in circular form, one should provide centre co-ordinates of the arc and the direction of the arc (clockwise/anti-clockwise).

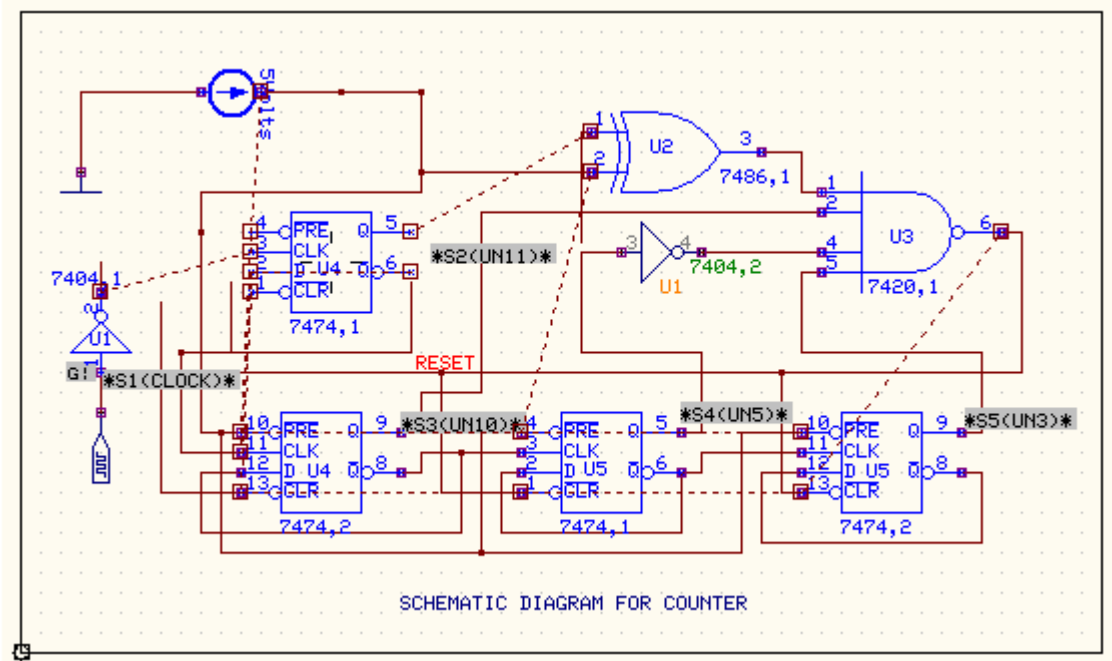


The output with same parameters and the Rotate Components option enabled is given in the figure below.



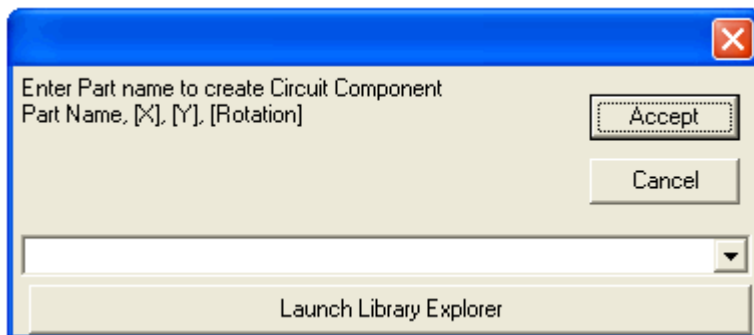
Highlighting of connected components

On selecting a component, those components which are connected to it are highlighted. This feature works when the option tool Display connected components is ON in the Relocate Component function tool.



Launched Library Explorer in the Add Components by name dialog

Added Launch Library Explorer button for easier provision for loading of components



Enhanced Block component option in Relocate by vector.

Earlier, Block component option relocates only components in the block. Now it is enhanced to relocate connections along with components in the block.

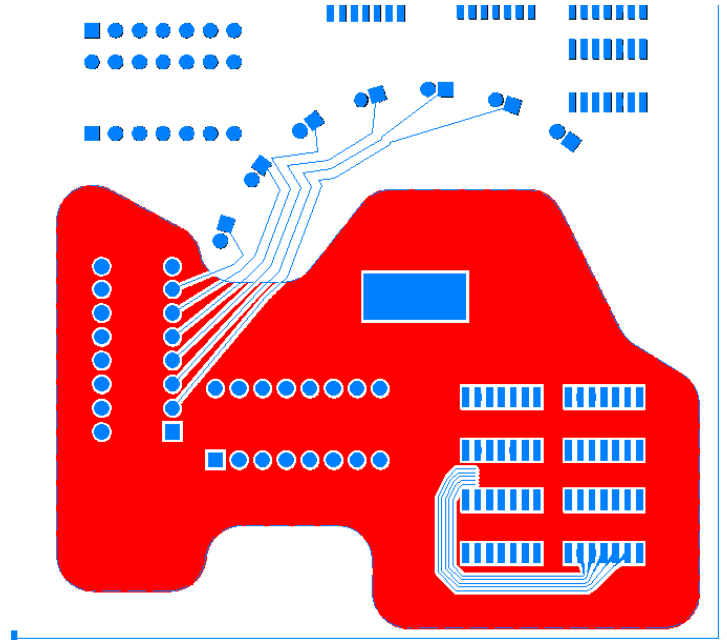
Instant packaging enhanced:

Previously only first symbol placing will be packaged and it stops there. Each symbol should be loaded by typing the name or from explorer. But now this is modified in such a way that symbol is available at mouse cursor after placing the current one.

Layout Editor

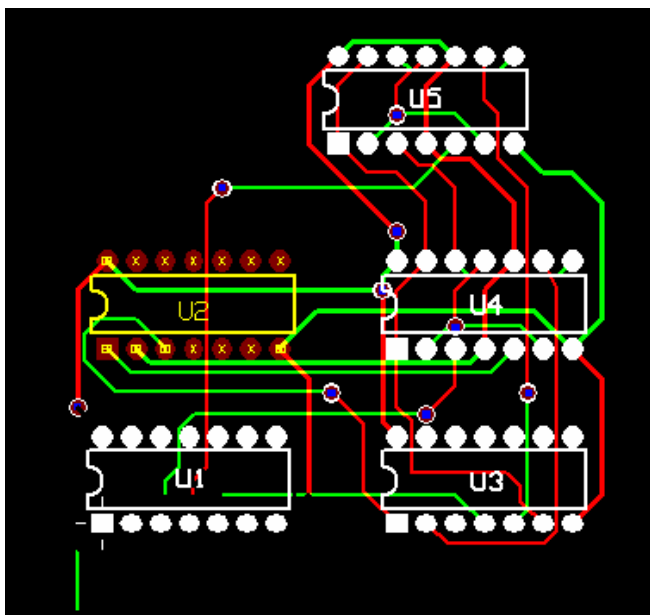
Round Mitered Polygon

Now it's possible to change the pointed vertices of polygon to rounded polygon by inserting arc. Now this option is implemented in Copper section also. For this select the stretch item function tool in Copper and select insert round miter option tool. Now clicking on a polygon vertex the radius popup band appears. Choose the appropriate radius; the pointed vertex will get replaced with an arc of specified radius. Also remove miter and remove arc options are available. The remove miter option deletes the arc and the polygon vertex appears as it was before inserting arc. When option remove arc is taken and click on an arc vertex, the arc get replaced with a line linking the end points of arc.



Highlighting of connected components

On selecting a component, those components which are connected to it are highlighted. This feature works when the option tool Display connected components is ON in the Relocate Component function tool.



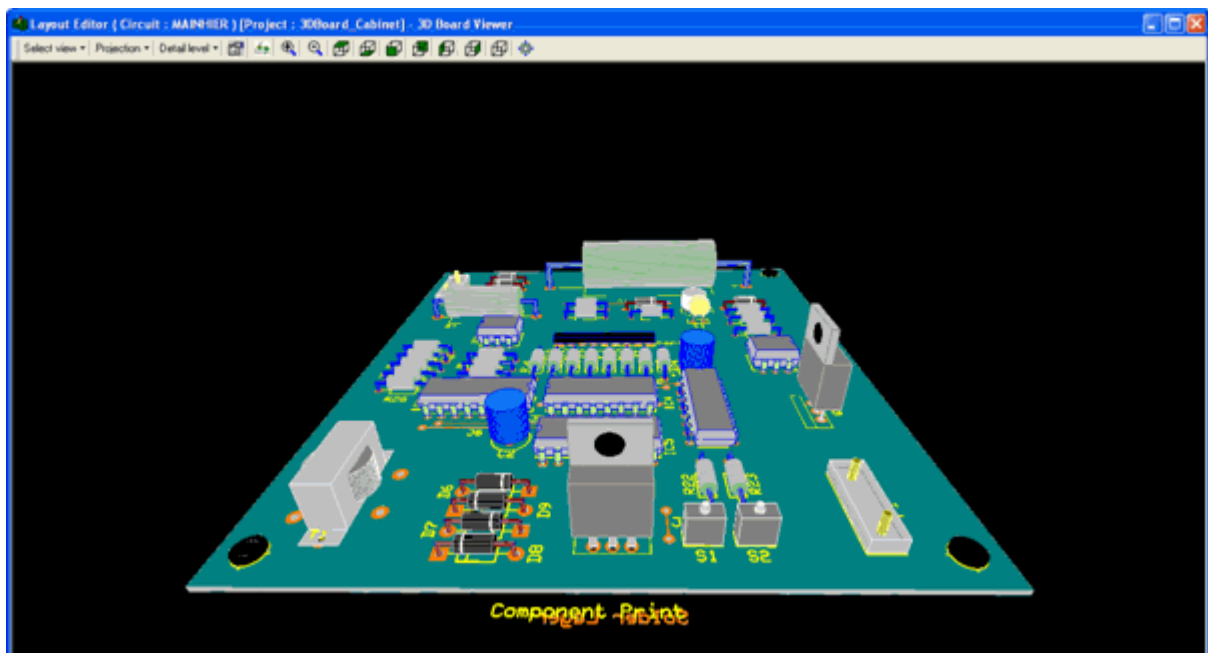
New 3D Viewer using OpenGL

When this tool is invoked, a separate Layout viewer will be opened which contains the 3D board view of the project. The board can be rotated with the mouse buttons.

Moving mouse up and down with depressed left mouse button rotates view around X axis.

Moving mouse left and right with depressed left mouse button rotates view around Y axis.

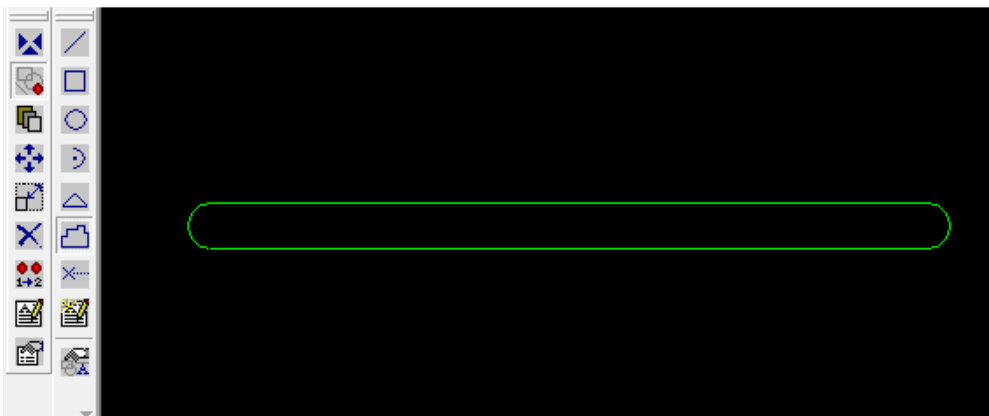
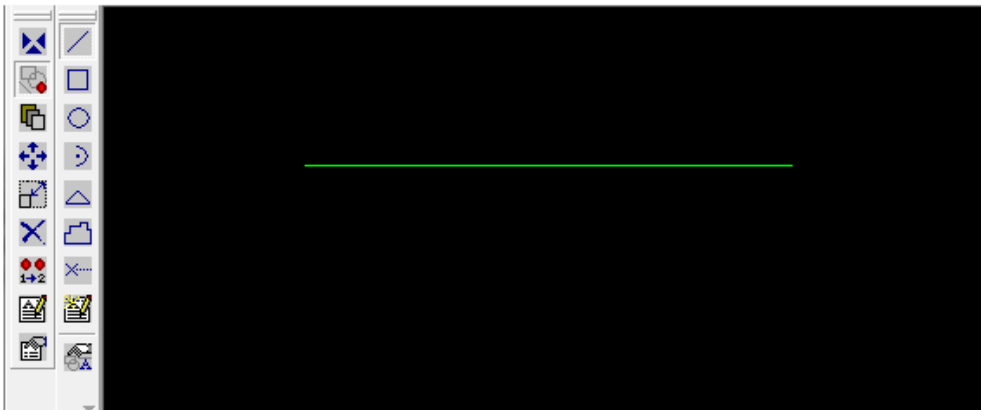
Moving mouse left and right with depressed right mouse button rotates view around Z axis.



Library Editor

Convert line/arc contour to polygon

Contour of arc/line can be converted to a polygon. The polygon created will be exactly the same size and shape of contour of that line. There will be two arc segments at both ends connected by two line segments. This contour polygon has all property similar to a polygon in EDWinXP. When creating the polygon from the contour of line, it creates a polygon having seven vertices and for polygon from contour of arc, polygon with nine vertices will be created.



Part Creation using Script

Part Creation using Script is a new feature in Library Editor Module. Using script part creation can be simplified. We can create a new part or edit an existing part by scripting in the Part Script Editor.

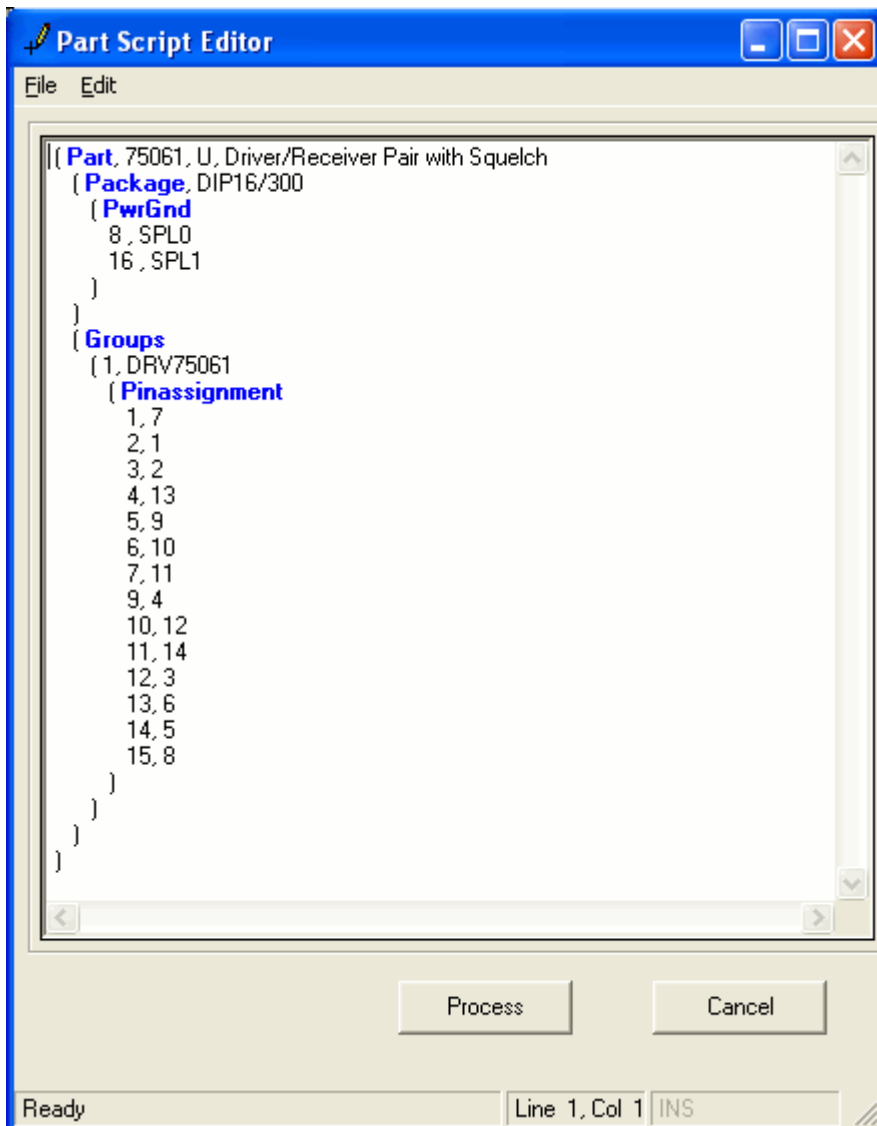
Syntax for the script is as,

```

{ Part, PartName, Prefix, Description
  { Package, PackageName
    { PwrGnd
      PackagePin , PwrGndName
    }
  }
  { Groups
    { GroupName, SymbolName
      { Pinassignment
        PackagePin, #Symbol Entry or Symbol Entry Name
      }
    }
  }
}

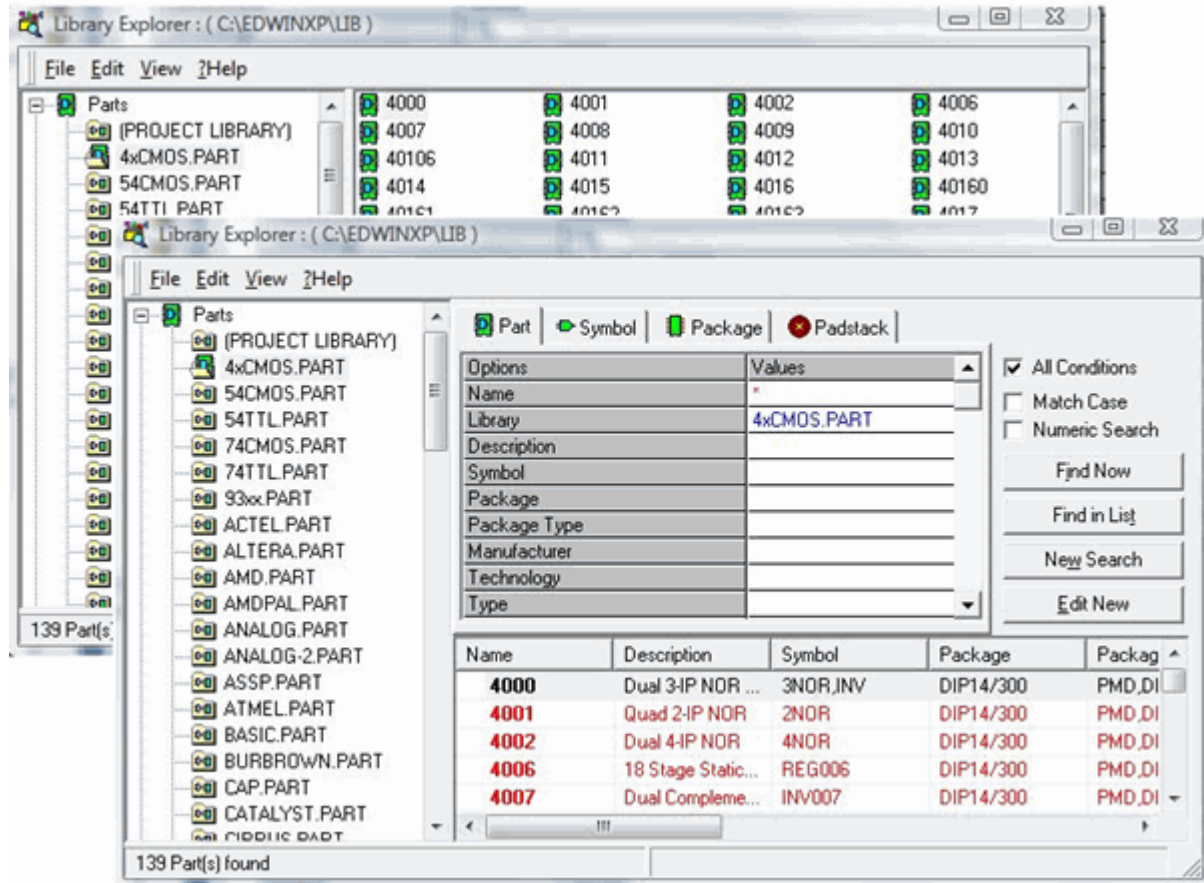
```

On selecting the Edit Script option in the Edit Menu in Part Edit Tab, a scripting window will pop up with a template, if any part is opened then the script for that part will be on the scripting window. Write/Edit script in the correct syntax and process it, then it will display the errors and warnings if any.



Library Explorer and Library Browser combined

Library Explorer and Library browser combined to single application to enable search and exploring components much easier. The new application will be named as EDWinXP Library Explorer.



[What's New in EDWin XP1.71 - **Schematic Editor**](#)

[What's New in EDWin XP1.71 - **Layout Editor**](#)

[What's New in EDWin XP1.71 - **Library Editor**](#)

[What's New in EDWin XP1.71 - **Fabrication Manager**](#)

[What's New in EDWin XP1.71 - **General**](#)

[What's New in EDWin XP1.70 - **General**](#)

[What's New in EDWin XP1.70 - **Schematic Editor**](#)

[What's New in EDWin XP1.70 - **Layout Editor**](#)

[What's New in EDWin XP1.70 - **Library Editor**](#)

[What's New in EDWin XP1.70 - **Fabrication Manager**](#)

[What's New in EDWin XP1.70- **New Libraries**](#)

Schematic Diagram Editor

—

Multiple Component Relocation

It is now possible to relocate a group of individually selected components (bulleted with Ctrl key + click). This option has also been implemented in Layout Editor.

Rotate and Relocate by selected Entry

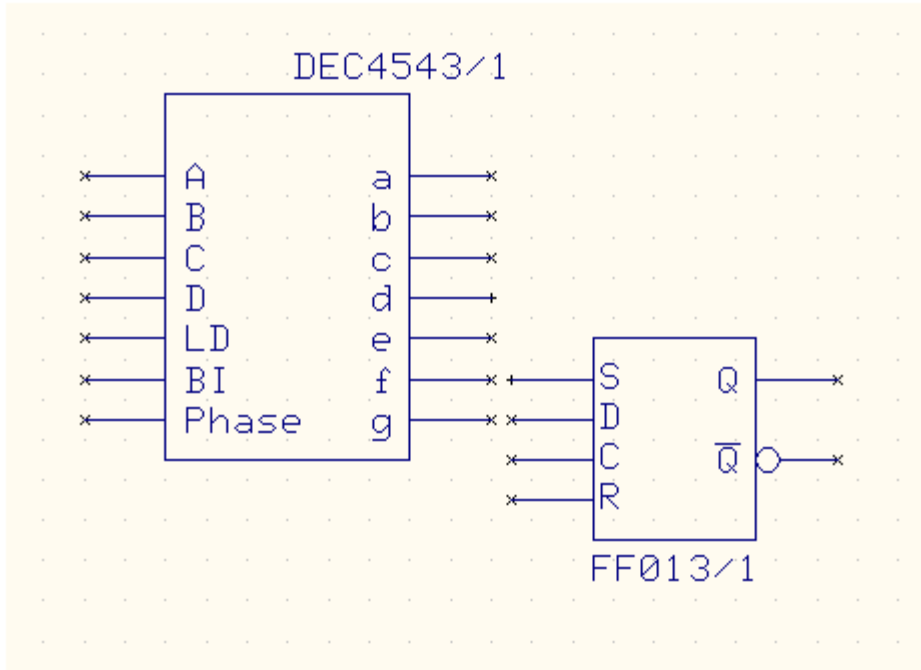
In previous versions, relocated components could be rotated only around entry #1. Now they are rotated around selected entry or (if element of the outline has been clicked for selection) around component's centre. In the later case, component's centre is used as the handle for relocation. This option has also been implemented in Layout Editor.

Selective Merging of Nets

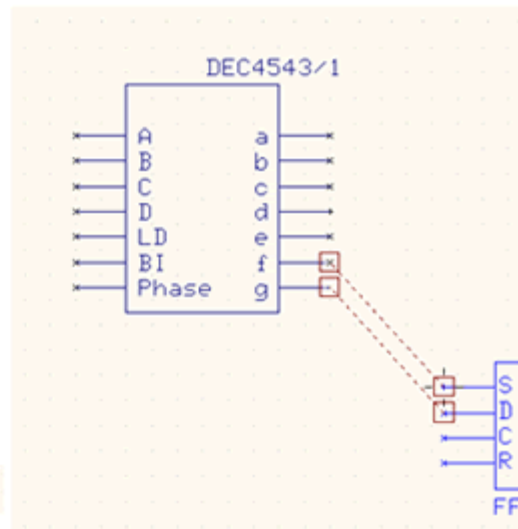
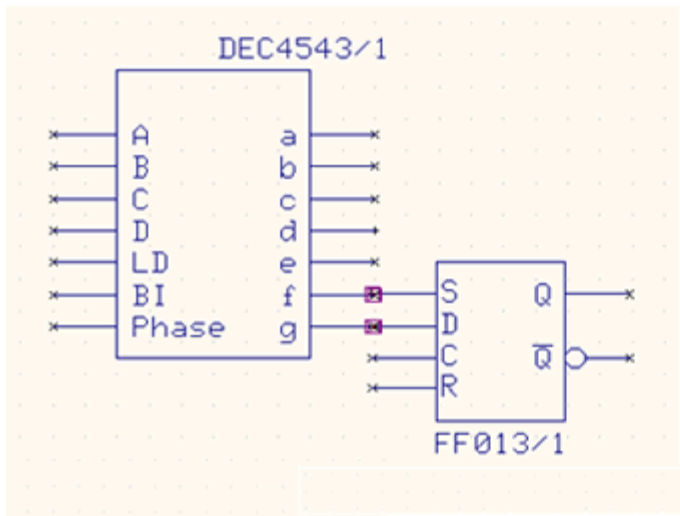
There is a new option for merging nets after block copy. Previously, merging of net with matching names could be executed either for Power/Gnd type nets only or for all nets. Now, the third option allows for individual selection of nets to be merged. This option is also available in Layout Editor

Overlap to Connect

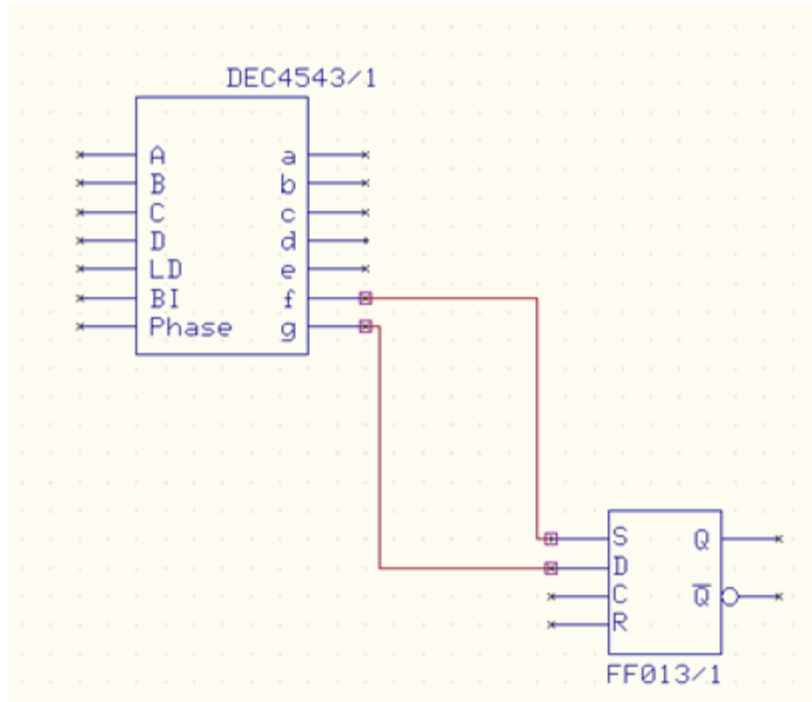
Connecting components in the diagram can be speed up by using new option "Connect by overlapping". This option applies to relocated components. Connection is made simply by overlapping pins that should be connected. See example below:



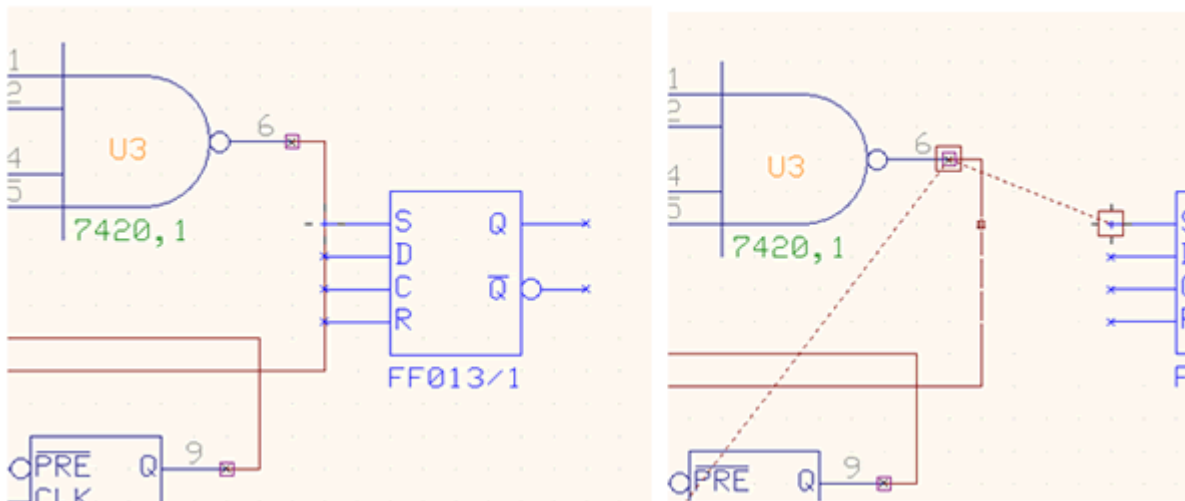
Let us assume that inputs 'S' and 'D' of relocated right hand component have to be connected to outputs 'f' and 'g' of the left hand component. Clicking left mouse button when right hand component has been relocated to a position where the pins to be connected overlap, results in creation of two new connections:



In the next stage, when the relocated component is placed at its final location, the connecting wires will be automatically routed:



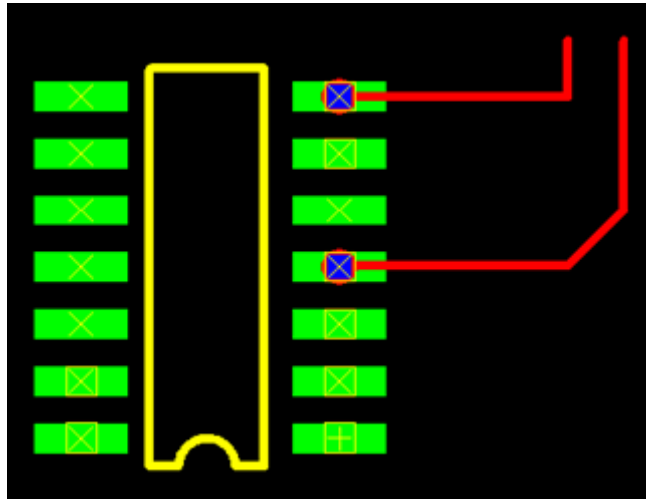
Similar effect can be achieved by overlapping wire segment with component pin selected as relocation handle:



Layout Editor

Automatic Insertion of Blind Via Holes

Option for automatic insertion of blind via holes when connecting trace from opposite or inner layer to an SMD pad has been added:

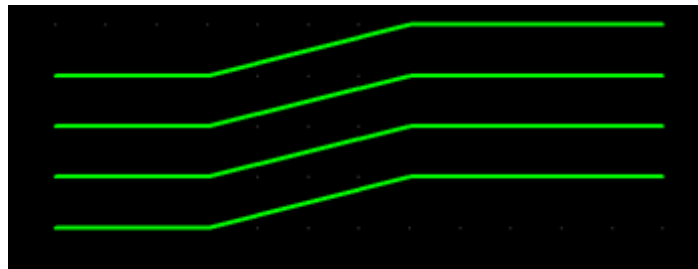


Edit Via Block

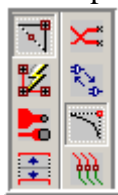
Previously, assigning/changing padstacks for via holes could be done only by single selection. In 1.71 this can be done by selecting via holes in block

Arc fitting

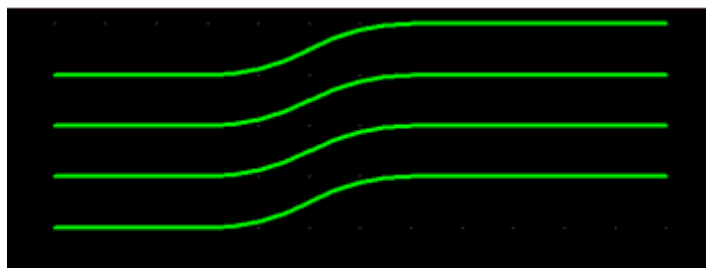
Arc fitting – a useful feature when designing flex boards. Trace prototypes may be routed in following fashion:



After selecting function, “Edit connection” and option “Arc miter at B Point”:

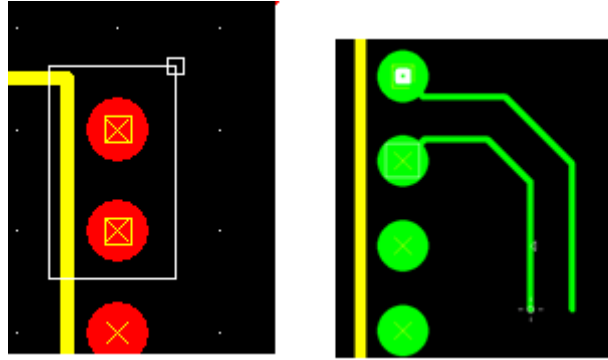


Click on selected ends of trace segments produces the following results:



Parallel Routing of Traces

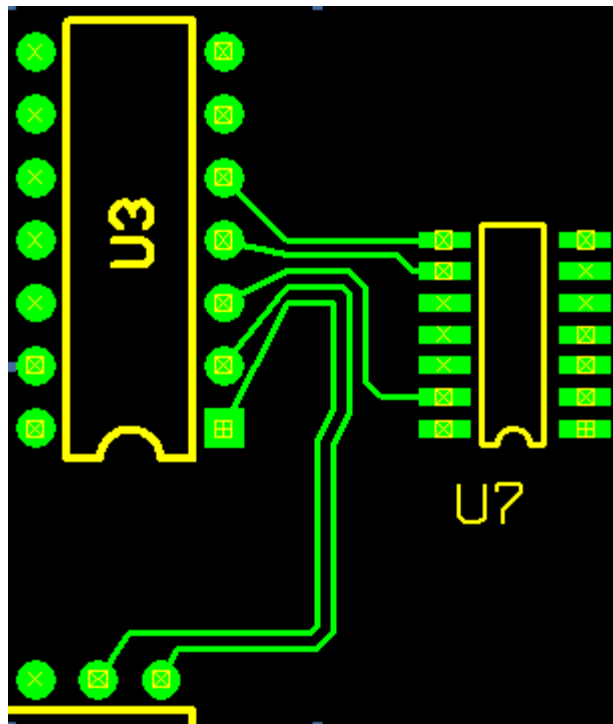
Parallel routing of traces has been added specially for routing differential pairs. Depressing key combination “Shift E” prior to selecting a starting pad of a traces sets the mode for blocking several pins:



The pad that is closest to origin of the blocking rectangle is taken as starting point of the leading trace in parallel group. In above example this will be the lower pad. The leading trace may now be routed and other traces will follow parallel with specified spacing. After arriving to final destination for the leading trace, it can be connected in normal fashion, whereas, the last segment of next parallel trace may be dragged to its own final destination.

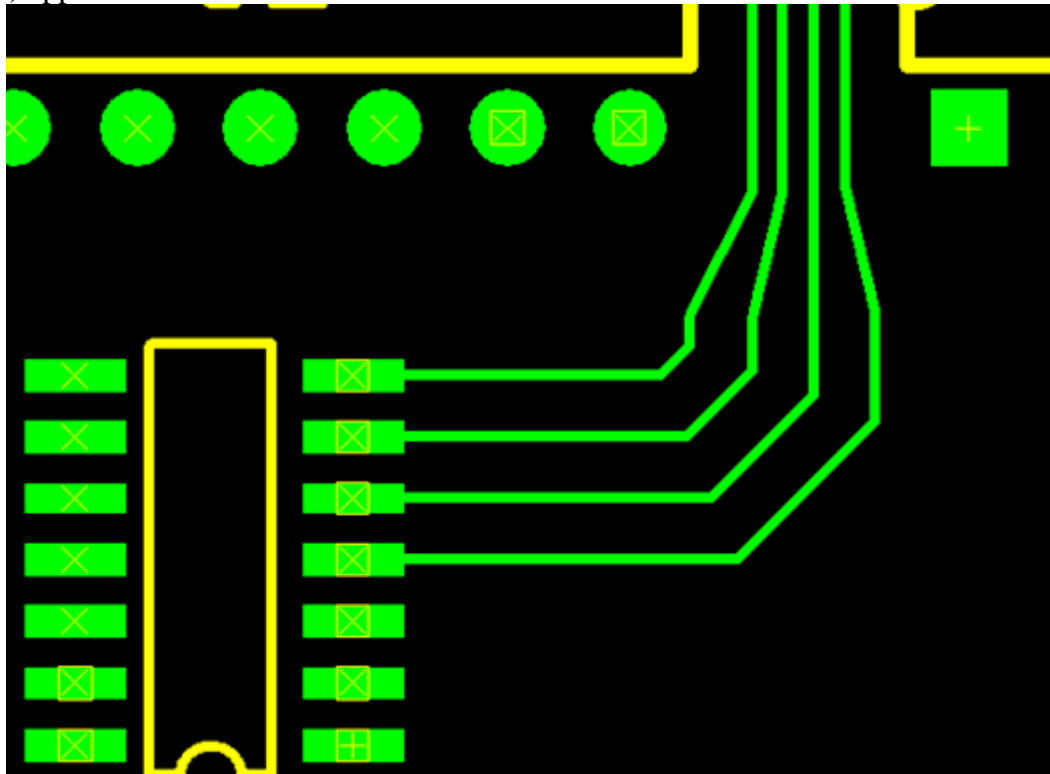


Up to eight parallel traces may be simultaneously routed using this method. When leading trace is connected, the next unconnected is taken as the leading and parallel routing continues until all in the bunch been connected or operation aborted by Esc. This principle allows for parallel routing of patterns like bellow



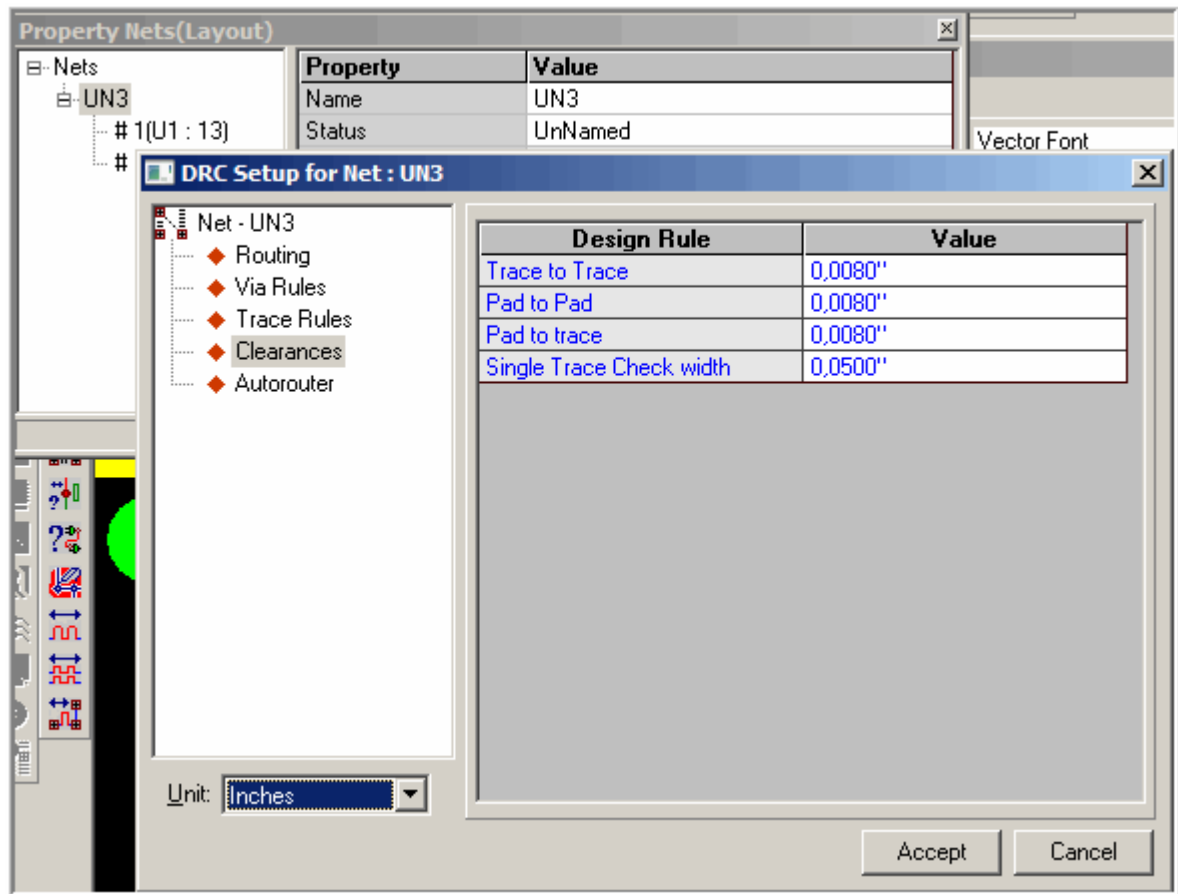
In some instances, it may be needed to narrow the spacing between traces to get through a tight spot. In such cases, routing of the leading trace and parallels may be terminated at any point with F4 key. With option "Allow T-connections" ON, lose ends of previously routed parallels may be grabbed in similar fashions as pads by blocking and new spacing (smaller or

bigger) applied:



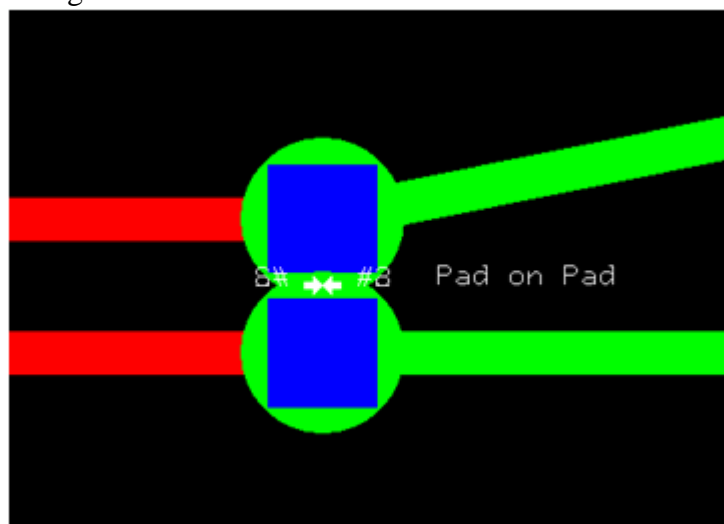
Setting Clearance for group of nets

Several users requested option to set clearance restrictions individually for a net, net group or class of nets. This possibility has been implemented in 1.71:



Display of Violation Description

Clearance violations were marked on the graphic screen by <- #violation type code, which required remembering what the code means. Now it is possible to get full violation description by hovering cursor over the marker:

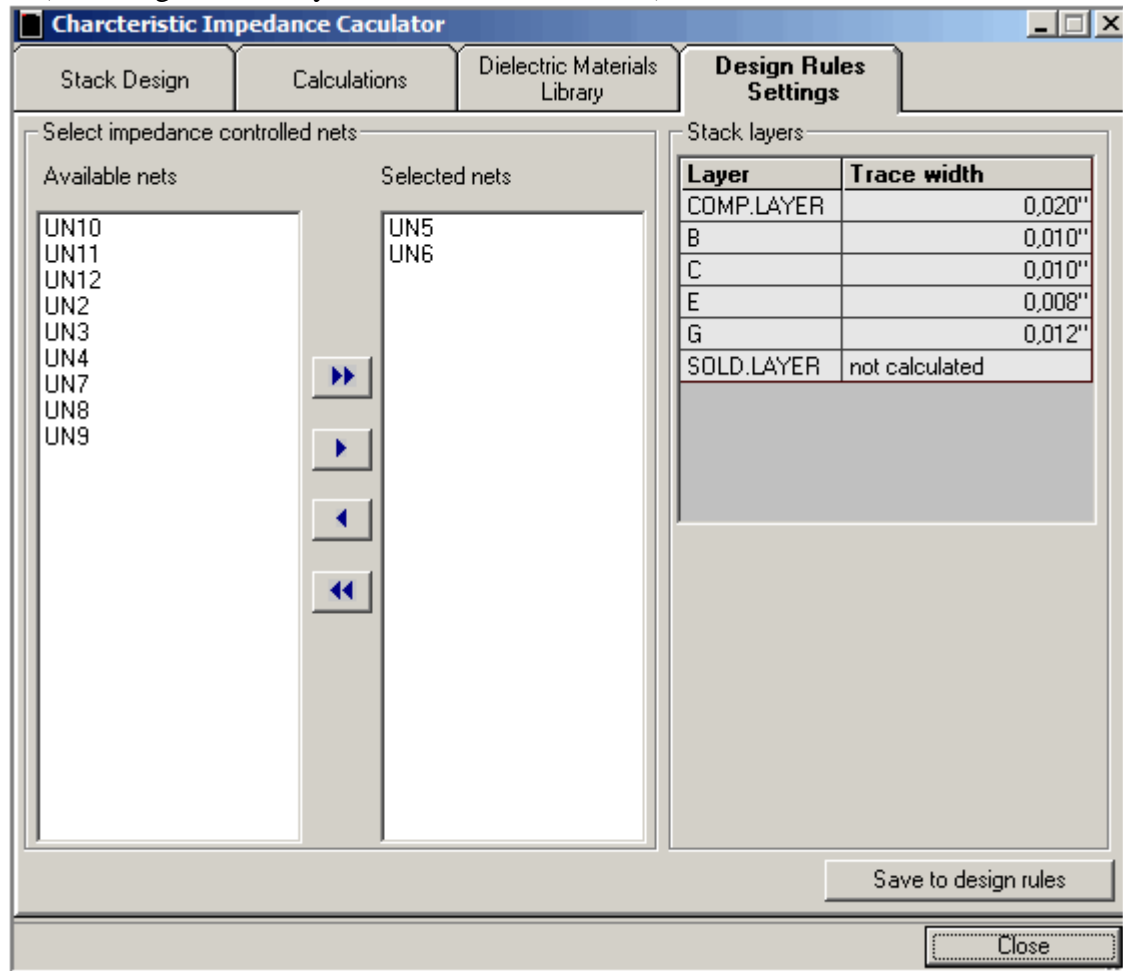


Step Rotate and Repeat for Copper, Board cutout outlines...

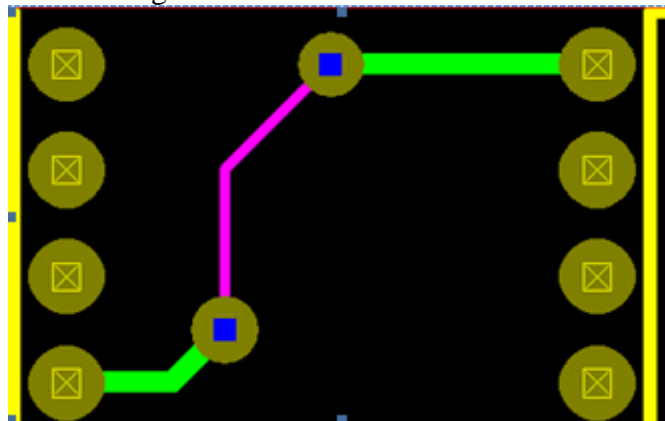
“Step and repeat item” and “Rotate & Repeat” options have been added for editing copper, and board cutout outlines. Repeat options apply to copper pour/copper relief polygons too. They are also implemented in Fabrication Manager.

Design Rules Settings in Characteristics Impedance Calculator

Optimal trace widths calculated with help of impedance calculator for every layer in the stack, may be stored as design rules. These rules will apply for all nets that have been assigned status “impedance controlled net”. This assignment means that whenever a trace for impedance controlled net is routed, the trace width will reset to width set for currently routed layer (assuming that this layer is included in the stack):

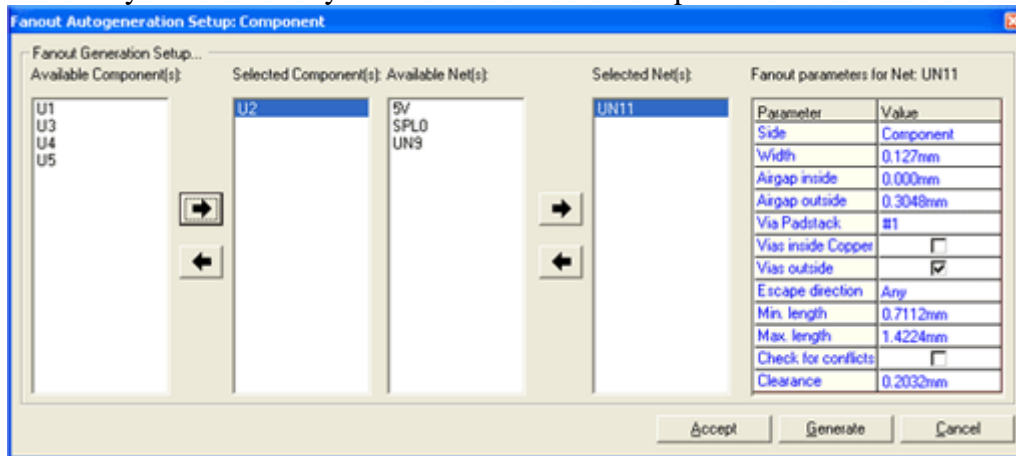


As in above example, the optimal trace width calculated for COMP.LAY was 0.020". This width is automatically assigned to trace segment originating on this layer. After layer change to "B", trace width switches automatically to .010". Returning to COMP.LAYER causes automatic change of the trace segment width back to .020":



Automatic Fan-Out Generation of Selected Components:

Previously, the selection for automatic fan-out generation had to be made net wise. In 1.71, this function may be additionally restricted to selected components.



Importing Session files in SPECCTRA

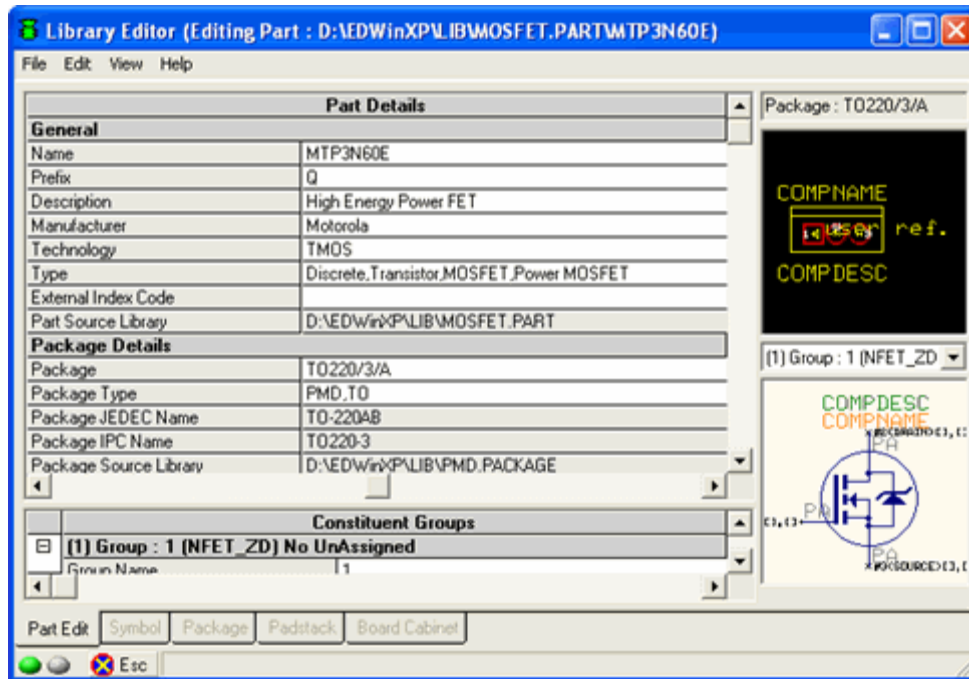
By adding possibility of importing files in DSN format (session files), EDWinXP user can now autoroute boards with help of <http://www.freeroutings.net> and Electra auto routers.

Library Editor

IPC-7351 Land Pattern Naming Conventions of Packages

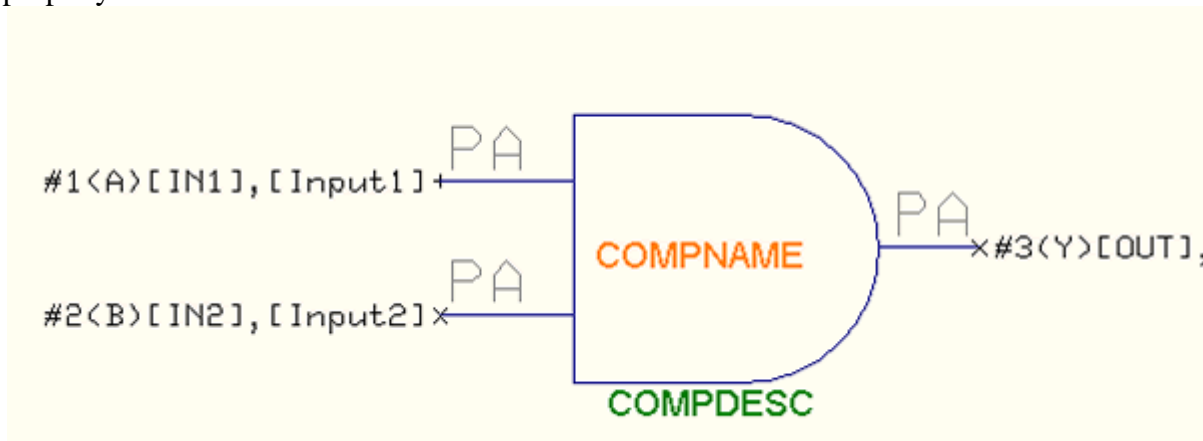
The IPC-7351A standard provides an intelligent land pattern naming convention that aids in communication between engineering, design and manufacturing. It specifies information on attributes such as component family, pin pitch, pin quantity, lead span etc.

Package names according to IPC-7351 Land Pattern Naming Convention standards have been added as additional package property for all elements in system libraries. IPC names can be used as search keys for browsing and searching libraries and will appear in output from List Generator.



Enhanced Display of Schematic Symbol Entry Names

Display of entry names in schematic symbols has been extended by MM Simulator and EDSpice pin assignment. This allows for instant check whether edited symbol has been properly set for simulation.



Enhanced Property Dialogs

The properties dialog of entries, padstacks, items, and texts in library editor are being auto covered. System recognizes automatically which type of Property dialog should be displayed depending on what type of item has been clicked on the screen. Previously it was controlled by setting tool options. These superfluous buttons have been removed

- **Entry properties dialog**

The Property dialog to show entry properties has been enhanced with new features to change entry name, view symbol's Mixed mode value, change mixed mode entry name, view symbol's EDSpice value, change EDSpice entry name. Now Entry name, MM Simulator and EDSpice entry values can be changed within the enhanced entry property dialog. **Padstack Properties dialog**

The Property dialog to show padstack properties has been enhanced with a new

feature to add new padstack to the padstacks list so that the changing of padstacks can be done in an easier way within the dialog. New padstacks can be added to the list and can be assigned to the desired pad easily from the properties dialog.

- **Symbol Properties dialog**

There is a functionality improvement in symbol properties dialog. The selected Mixed mode or EDSpice simulation model's entries will be automatically assigned to the symbol from the first pin in an incrementing order. Thus manual way of entering simulation names is not necessary now. Editing of simulation entry values can be done manually in a preferred way from the entry properties dialog

New Components in Library

About 50 specially requested parts have been added to system libraries.

No.	PART	SYMBOL	PACKAGE
1.	1367073	CONN1367073	SMD20/A
2.	25K2231	NMOS2231	TO3/4/A
3.	3002	BATHOLD3002	SMD3/A
4.	9WAYCONNECTOR	CONN/9	CON/HEADER9/A
5.	AD5328	DAC5328	SOP16/170A
6.	ADXL323	SNS323	QFP16
7.	ADXL330KCPZ	SNS330	LFCSP16
8.	AM-HRR3-315	Rx315	SIP15/DS/P10
9.	AM-RT5-315	Tx315	SIP7/DS/P4
10.	ASSR1218	RLY1218	SOP4
11.	AT45DB321D	MEM321	SOIC8/150
12.	ATA6660	TxRx6660	SOIC8/150
13.	ATmega32U6-AU	MCNTRLR32U6	TQFP64
14.	ATmega32U6-MU	MCNTRLR32U6	QFN64
15.	B3U-1000P-B	SWITCH	SMD2/A
16.	CSTLSMGxxx-A0	RESNTR	SIP3/DS/B
17.	DSPIC33FJ64MC804	MCNTRLR804	TQFP44/D
18.	FFCCON	CONN/FFC8	CONN/FFC8
19.	FTR-120-01-S-D	CONN	CON/HEADER20/SM
20.	FTR3-P3CN010W1	RLYP3CN010W1	RELAY5/C
21.	L165	OPAMP165	DIP5/B
22.	LM2700MT	CONV2700	SOP14/170/B
23.	LPC1766FBD100	MCNTRLR1766	QFP100/J
24.	LPC2368FBD100	MCNTRLR2368	QFP100/J
25.	LPC2478	MCNTRLR2478	LQFP208
26.	M4822M1V	RAM4822	DIP36/600
27.	MAX355CWE	MUX355	SOIC16/300/C
28.	MAX9110EKA-T	DRV9110	SOT23/8
29.	MAX9111EKA	Rx9111	SOT23/8
30.	MBI1802	DRV1802	SOIC8/150/B
31.	MCP6522	OPAMP6522	DIP8/300/C
32.	MCP9700AT	TMP5NS9700	SOT23/5A
33.	MIC5014BM	DRV5014	SOIC8/150
34.	MP4212	MOSFET4212	SIP10/DS/A
35.	OP400	OPAMP400	SOIC16/300/D
36.	PC1602ARU-HWB-G-Q	LCD1602	DIP16/100
37.	PIC16F677-I/SO	MCNTRLR16F677	SOIC20/300
38.	PIC16F684	MCNTRLR16F684	SOIC14/150
39.	PIC16F884	MCNTRLR16F884	TQFP44
40.	PIC16F886	MCNLR16F886	DIP28/300/A
41.	PIC18F4620/P	MCNTRLR18F4620	DIP40/600
42.	SCDA4A0301	CONN16	CON/16/SMD
43.	SMCONN	CONN	CON33/SMD
44.	TL750LD	VREG750	SOP8/150
45.	TLC272CD	OPAMP,OPAMPA	SOIC8/150
46.	TMC223	DRV223	QFN32
47.	TMC249/A	DRV249	QFN32/A
48.	TMC454	CNTRLR454	BGA144
49.	TPS2829DBVT	DRV2829	SOT23/5/D
50.	TRIMMERCAPACITOR1	CAPVAR_1	CVAR3/A

Fabrication Manager and Fabrication Graphics Viewer and Import

Apart from general improvements for graphic screen control (that has been mentioned above) changes in these two applications apply mostly to graphic imports.

Enhanced Fabrication Graphics Viewer

DXF import

It has been brought to our attention that users designing flexible boards wish to import trace

patterns (artworks) drawn with the help of mechanical CAD Packages. They needed DXF import to artworks layers in true size line width. In previous version, DXF import was intended for importing outlines only and line width were ignored. It has been changed in 1.71 and now DXF can be imported to all layers, except Drill Template.

Aligning Imported Layers :

There is a tool in Fabrication Graphics Viewer for aligning imported layers. Aligning may not be necessary if all layers and drills are imported with import parameter “Original coordinates” set to ON (see Import Parameters dialog). Nevertheless, aligning tool has been retained since auto alignment may work only if graphics in import files have the same origin.

Distribution of Graphics to Import categories:

Since release of 1.70, the Fabrication Graphics Viewer replaced previous ports for importing graphics for project reconstruction (reverse engineering). In this task, the main problem is proper distribution of graphics to import categories (traces, pads, pad position). This is due to ambiguity of graphics imported in supported formats.

Basic distribution to import categories is done automatically when graphics are transferred from the viewer to Graphics Import editor in Fabrication manager. Some internal code changes have been made in transfer function, which should result in more exact categorization. Nevertheless, it can never be ensured that this distribution would be 100% correct. Usually some inter-category transfer of element is required.

This task was possible before in Graphics Import editor, but since it had to be done through Property Dialog, the process could be very laborious. In 1.71, a tool has been added enabling direct transfer from category to category of elements selected individually or by blocking.

Detecting DCODEs:

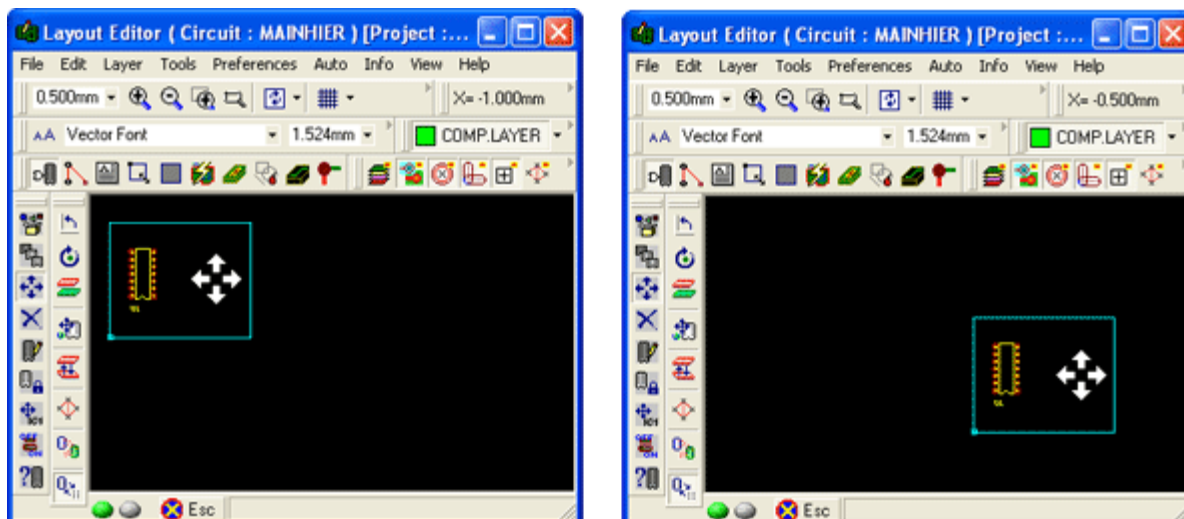
Options to enquire for Gerber aperture codes (DCODEs) have been enhanced. Even previously, all elements that were imported with the same aperture could be highlighted. It could have been done by clicking on column and row listing the aperture in Import Dialog, Filters section or in Layer Property dialog. Now the same may be done by clicking on element on the screen. In other words, enquire for Gerber aperture codes works now both ways; from aperture code to associated elements and from element to its aperture code.

General Improvements

Control of the graphic screen has been significantly improved by introducing following features:

Panning with Mouse Scroll Button

Panning by dragging the image with middle mouse button depressed.



Smooth Zooming

New, “smooth” zooming in and out with mouse wheel. This, and above feature apply to all screens where data is presented graphically.

Enhanced Dialogs

Dialogs controlling contents of the display – visibility of layers and import categories - have been made non-modal. Redraw with new settings is made instantly on request without necessity to close these dialogs. They may stay opened while user executes other functions. This feature allows for easier navigation through project elements.

Grid and Snap Improvements

Number of grid and snap values increased to 12

Bug Fixes

- Locking of zoom and pan functions in Schematic Editor upon launching auto placer. Problems in simulating Op Amp based circuits in EDSpice. Wrong display of schematic entry and gate assignment in component property window in Layout Editor. Enabled “Allow T Connections” option tool is disabled when ESC key is pressed during routing connection. Visibility of copper relief elements in Layout Editor restricted to “Meshed Copper Pour Areas display. Previously these elements were displayed always.
- Problems with generating model .dll for mixed mode simulator.

What's New in EDWin XP1.70 - General

Automatic detection of updates :

EDWinXP has been equipped with a function that automatically detects that updates are available and informs the user when program is invoked.

Storing/restoring settings:

All current settings may be stored and then restored in case of reinstallation of EDWinXP.

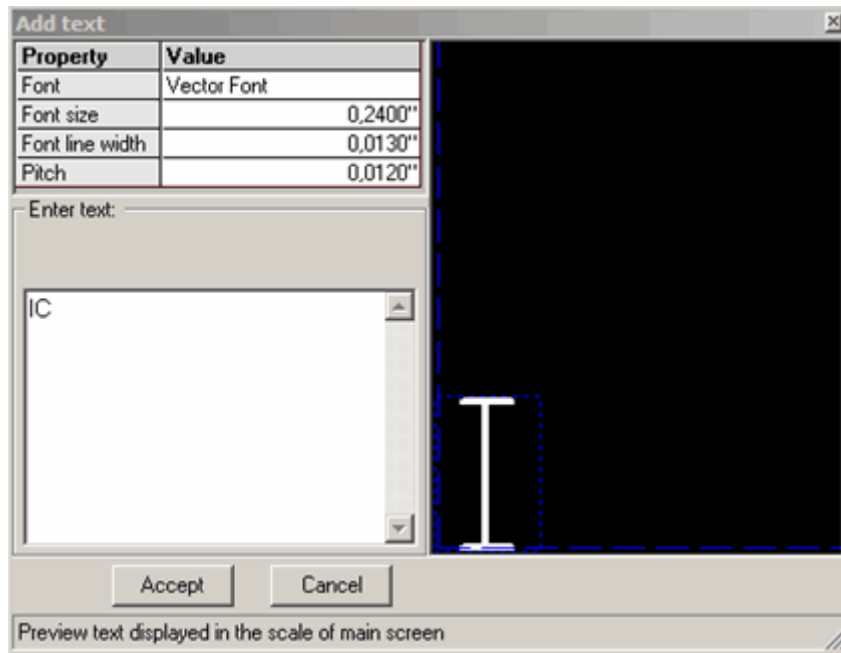
Remembering latest file path:

Whenever disk file is opened for output and input the file open dialog redirects to the folder selected with previous opening of a file of the same type.

New text input dialog with preview :

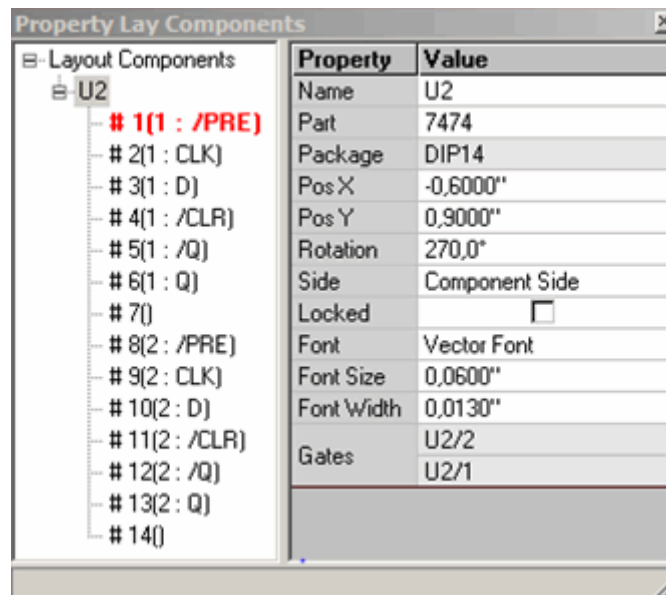
Several users wished that dialog for text input should show also text preview in the same form and size as on the graphic screen. The problem was in selecting proper text size in relation to the size of objects displayed on the main screen. In the new dialog, the first character of entered text is shown in preview screen in current scale of the main

graphic screen. Text preview dialog has been added to all applications where there is a need for entering text. Additionally, any required text size may be also set directly in this dialog. Previously user could select only one of 15 preset sizes. Possibility to preset text sizes for all editors has been though retained in order to facilitate fast selection. It applies also to setting text sizes in all Property dialogs .



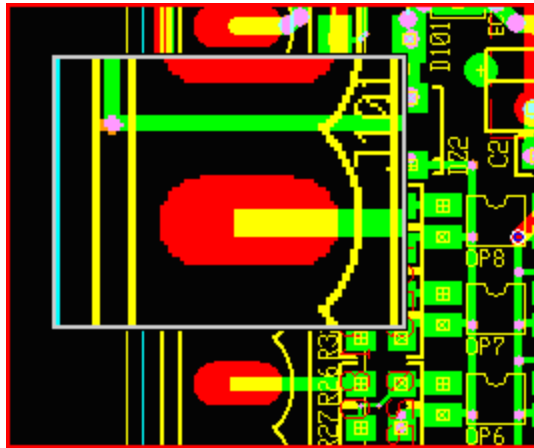
New color scheme for Property dialogs:

Most used form of dialog in EDWinXP employs a double column grid, accompanied in many instance by explorer type "tree view". Cells in left hand column are used to display names of properties or parameters. Values are presented and entered into cells of right hand column. Not all values are changeable in such dialogs - some are presented only as additional information. User expressed difficulties in distinguishing which values are settable and which are purely informative. This problem has been addressed in 1.70 by introducing uniform color scheme for all such dialogs. Data may be entered only into cells with white background color. Those cells that are displayed with grey background color contain property names or values unchangeable by the user .



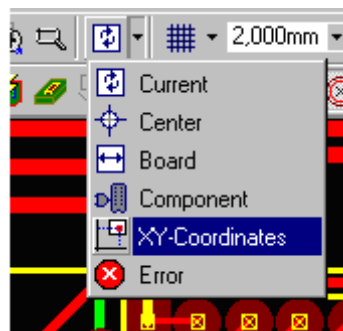
Magnifying glass:

All editors have been equipped with movable "magnifying glass". This feature allows viewing portion of displayed image in 1, 2, 3 and 4 x magnifications.



Coordinate Zoom :

Possibility to focus display on entered X, Y-coordinates has been added to redraw modes in all editors.



"Ruler" cursor :

Current cursor position is reciprocated in the ruler.



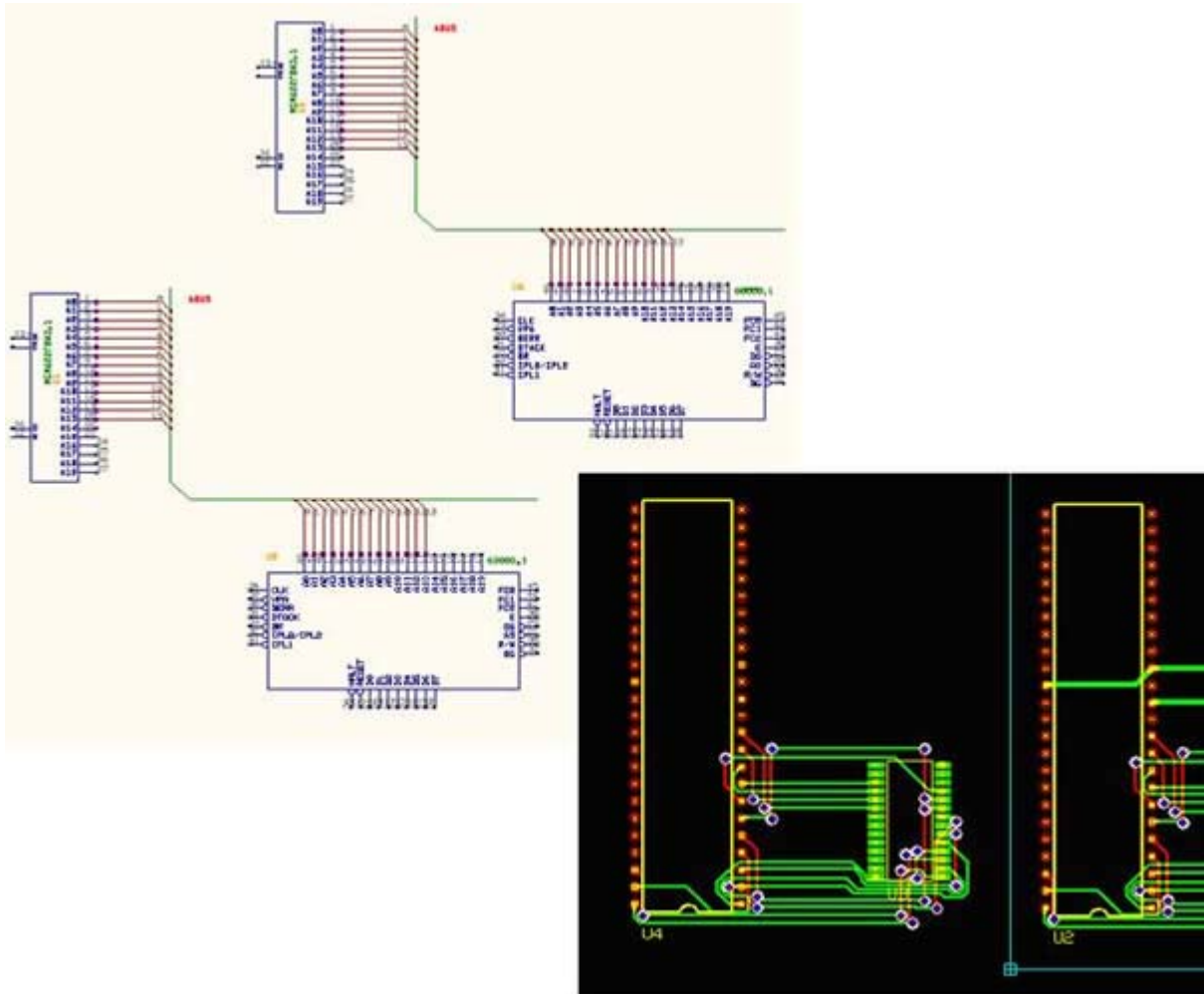
What's New in EDWin XP1.70 - Schematic Editor

Dual Copy and Paste function:

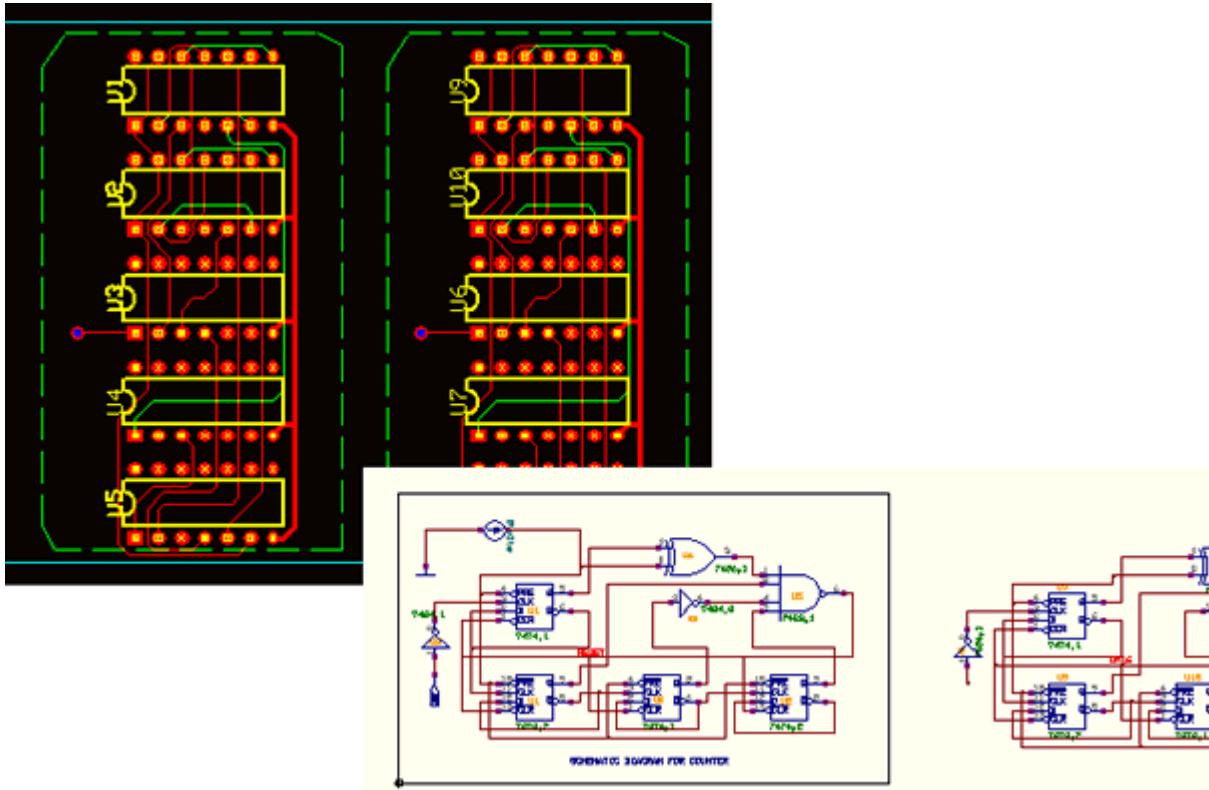
Since long time back, we have been asked to upgrade block copy/paste feature to allow copying parts of schematics with corresponding parts of PCB layout without losing topology of layout components placement and routed connections. The same applied to copying parts of PCB layout with maintained component positions and wiring on the schematic diagram. Previously, if block of schematics was copied, the layout part was not affected since copied schematics components were never packaged. Copying of buses was also not supported.

Block copy of PCB layout parts resulted in creating corresponding components on the diagram but they were stacked on top of each other and required laborious relocation to desired position on the schematic page. No wired connections were transferred. All above shortcomings have been fully solved in 1.70. Whenever block of schematics is copied and pasted, the program subsequently switches to Layout Editor allowing to relocate

corresponding block of layout (if there was any already edited) to its destination on the PCB.
Block copy function gives this effect only under condition that copied components were packaged and preference setting "Instant packaging" is ON.



Dual Copy and Paste works both ways. After copying part of PCB Layout program switches to Schematics Editor where resulting block of component and wires may be placed on currently active page. In cases when schematic component packaged in copied and pasted layout components were placed on different pages, their copies and copied wiring will be located outside of page outlines on respective pages. The interactive relocation of schematic part applies in any case to these components and wires that were originally placed on the active page. Nevertheless, placement topology of components and wires on hidden pages will be maintained.



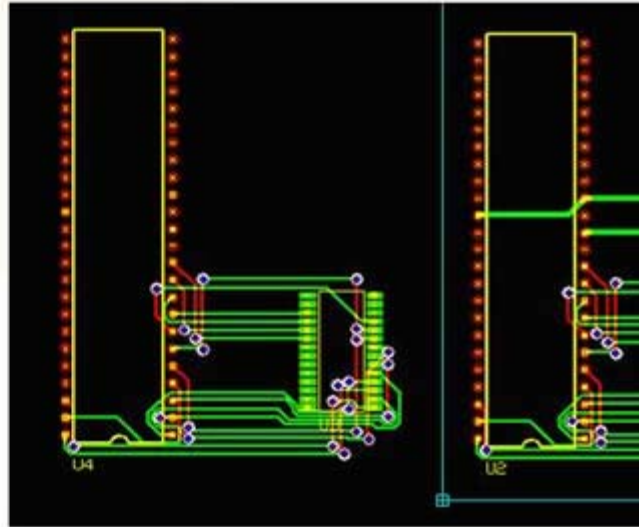
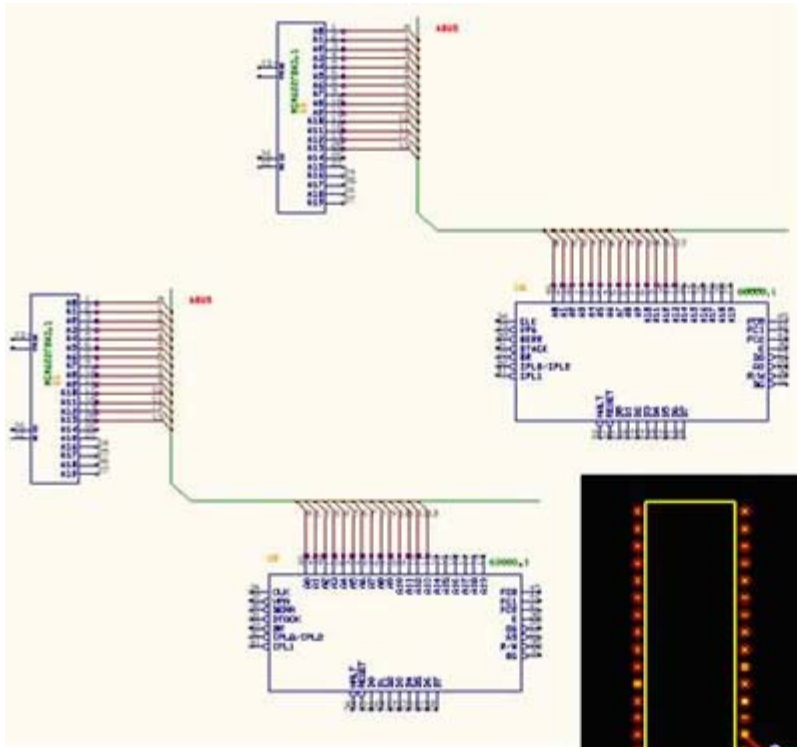
In other words, it does not matter anymore whether Copy and Paste operation was initiated in Schematics or PCB Editor - in both cases produced results will be practically identical .

"Switch to reroute" and "Rip up before reroute" options in Schematics Editor:
 These two useful options for manual routing of wires (similar to those implemented previously in PCB Layout Editor) have been now added to Schematics Editor.

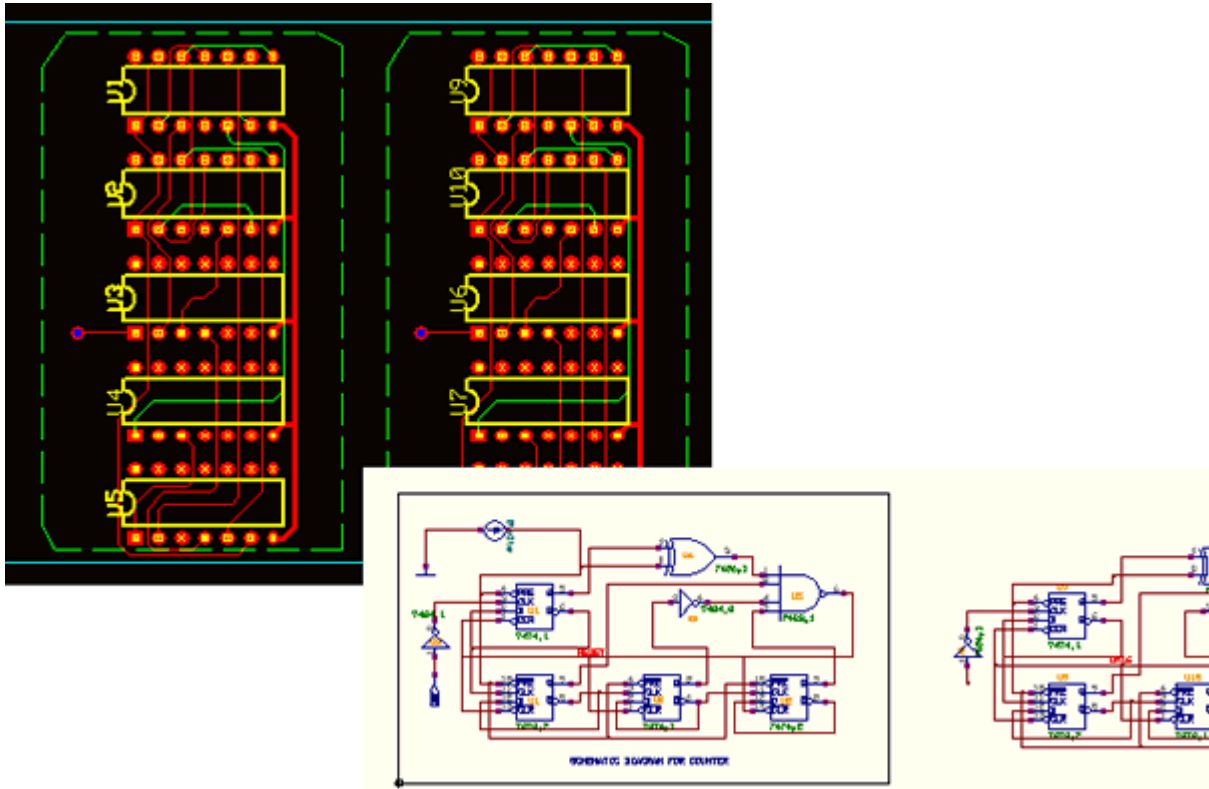
What's New in EDWin XP1.70 - Schematic Editor

Dual Copy and Paste function:

Since long time back, we have been asked to upgrade block copy/paste feature to allow copying parts of schematics with corresponding parts of PCB layout without losing topology of layout components placement and routed connections. The same applied to copying parts of PCB layout with maintained component positions and wiring on the schematic diagram. Previously, if block of schematics was copied, the layout part was not affected since copied schematics components were never packaged. Copying of buses was also not supported. Block copy of PCB layout parts resulted in creating corresponding components on the diagram but they were stacked on top of each other and required laborious relocation to desired position on the schematic page. No wired connections were transferred. All above shortcomings have been fully solved in 1.70. Whenever block of schematics is copied and pasted, the program subsequently switches to Layout Editor allowing to relocate corresponding block of layout (if there was any already edited) to its destination on the PCB. Block copy function gives this effect only under condition that copied components were packaged and preference setting "Instant packaging" is ON.



Dual Copy and Paste works both ways. After copying part of PCB Layout program switches to Schematics Editor where resulting block of component and wires may be placed on currently active page. In cases when schematic component packaged in copied and pasted layout components were placed on different pages, their copies and copied wiring will be located outside of page outlines on respective pages. The interactive relocation of schematic part applies in any case to these components and wires that were originally placed on the active page. Nevertheless, placement topology of components and wires on hidden pages will be maintained.



In other words, it does not matter anymore whether Copy and Paste operation was initiated in Schematics or PCB Editor - in both cases produced results will be practically identical .

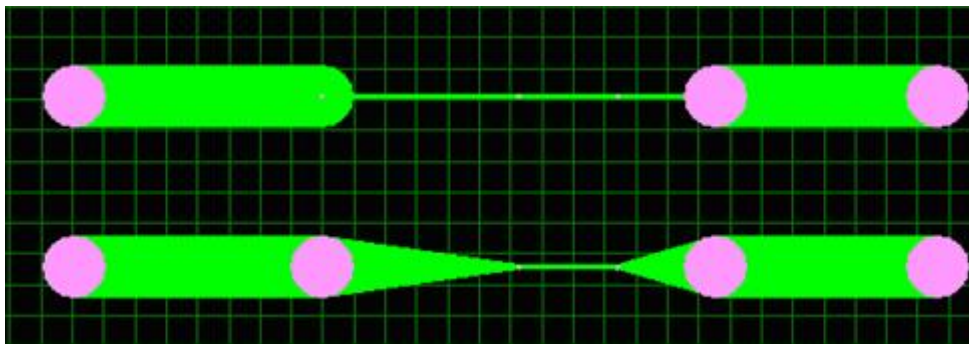
"Switch to reroute" and "Rip up before reroute" options in Schematics Editor:

These two useful options for manual routing of wires (similar to those implemented previously in PCB Layout Editor) have been now added to Schematics Editor.

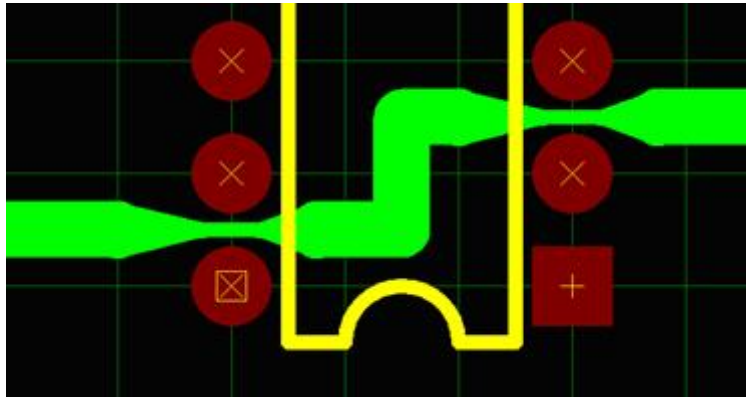
What's New in EDWin XP1.70 - Layout Editor

Apart of Dual Copy and Paste, several other user suggested features have been added to Layout Editor.

Tapered trace segments: Any trace segment may be assigned different widths at the start and at the end. When property "Tapered" is set at the beginning of a segment, it will produce following results:



If the width at the end of a segment is smaller then at the beginning, then the segment will taper down gradually along its all length. In opposite case, such a segment will taper up from smaller to bigger width. In version 1.70, this new feature has been used in several semi-automatic and automatic tools. User may for example force selected or all segments in any trace to taper whenever there is a change of width from segment to segment. This function creates smooth change of width in cases when thicker trace must be routed between pads:

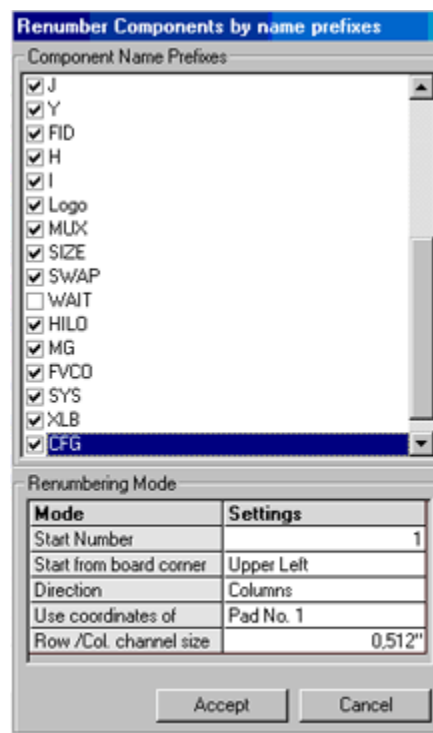


On request, all or selected trace segments may be automatically tapered to adjust to the size of the pad to which they are connected:

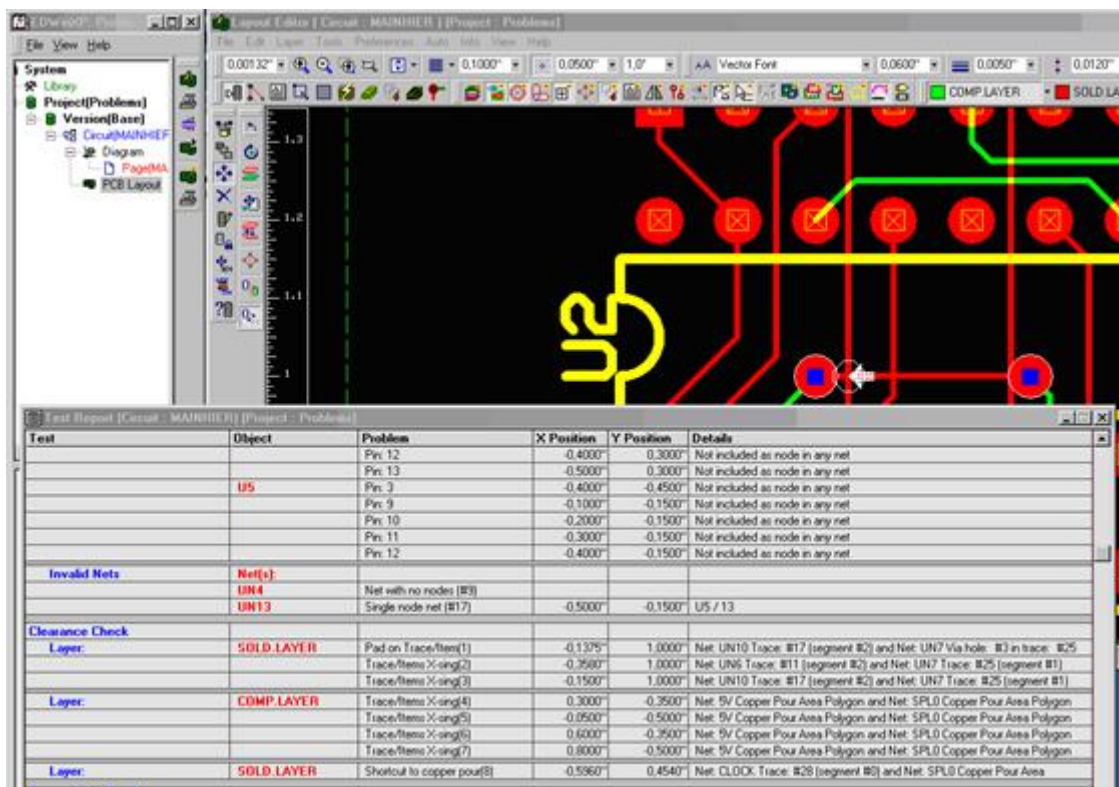
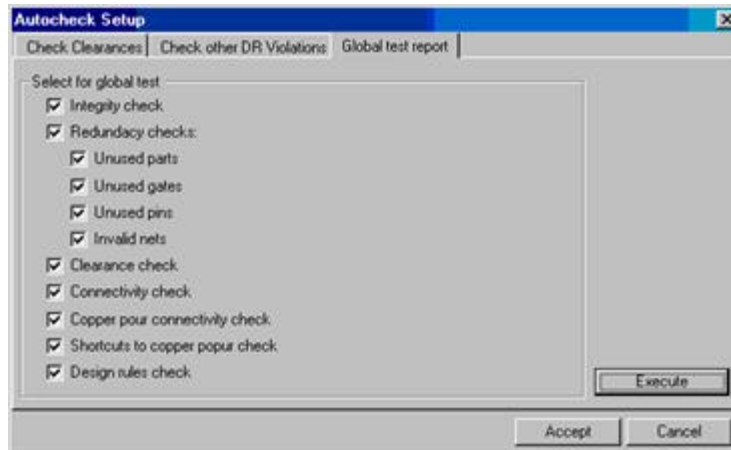


As seen on the picture above, ordering the thin trace segment to taper to a pad with bigger diameter produces similar results as creating "tear drop" pads by adding copper elements (a method used in previous versions of EDWinXP). The advantage of tapering is that there is no need to add any loose copper elements. The old method for creating "tear drop" pads has been retained for compatibility reasons .

Improved automatic renumbering function: In older versions of EDWinXP, automatic renumbering of components had to be executed by individually entering name prefixes. It could have been a very laborious process if there were many component name prefixes. It was also not easy to remember all name prefixes used in the project. In version 1.70, all prefixes are listed in the newly designed dialog allowing selection of all those that should renumbered. All components with name prefixes that were selected (checked) in the dialog are renumbered in one go .

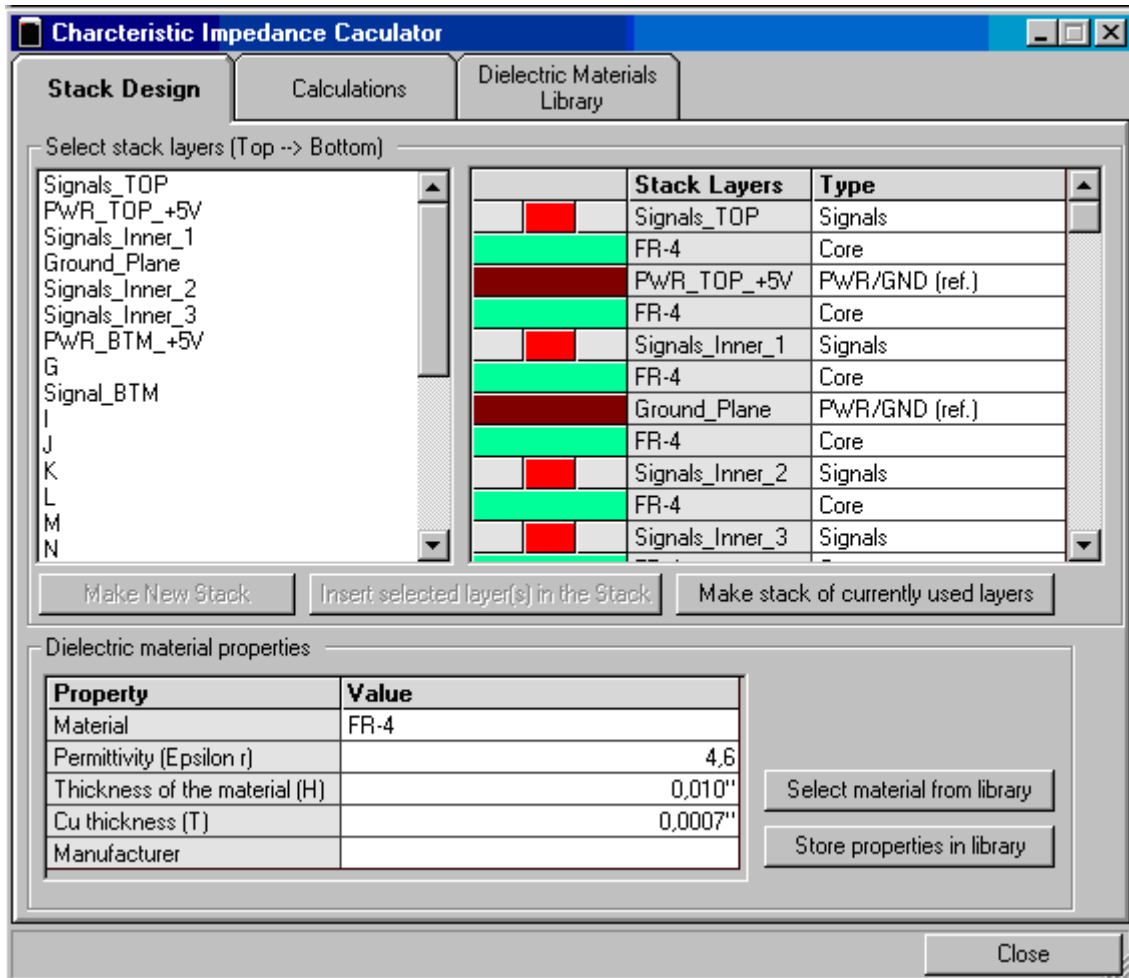


Global check and test report: Functionality of Layout Editor and Fabrication Manager incorporates all sorts of tests needed to ensure that a PCB was laid out correctly. All these tests and checks are designed to be executed individually. It may happen that running of some tests has been overlooked or the user missed significance of some tests for ensuring that particular PCB design is correct. Solution to this, introduced in 1.70 is global check that in one go executes all available tests in proper order and produces test report containing details of all detected problems. Mouse click on some problem listed the test report results in focusing image on the main screen on this problem and displaying a marker that points to its exact location.



For the record, the contents of the test report may be output to a disk ASCII file. .

Characteristic Impedance Calculator : This new tool allows designing layer stack (from available EDWinXP layers) and assigning layer type property (PWR/GND, Signals or Mixed).











Other parameters are permittivity of dielectric material, thickness of dielectric material, Cu thickness and planed trace width on signal layers. Program automatically applies suitable characteristic impedance formula depending on layer configuration. (Microstrip, Embedded Microstrip, Stripline and Dual Stripline). It is also possible to calculate required trace width for the layer when value of characteristic impedance is specified as a design rule.







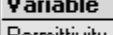
Characteristic Impedance Calculator

Stack Design **Calculations** Dielectric Materials Library

Select layer for calculations

Stack Layers	
	Signals_TOP
	PWR_TOP_+5V
	Signals_Inner_1
	Ground_Plane
	Signals_Inner_2
	Signals_Inner_3
	PWR_BTM_+5V
	Signal_BTM

Applicable formula

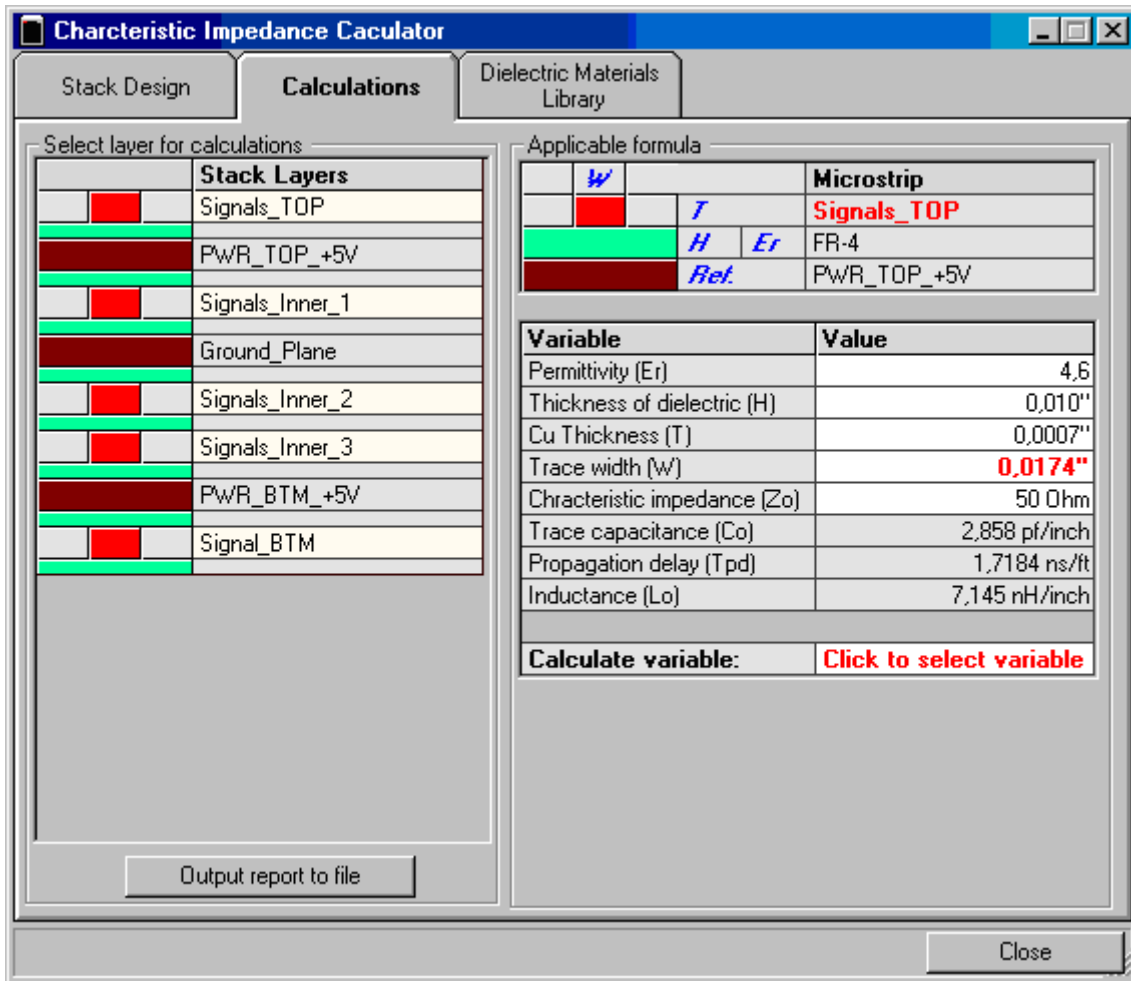
w		Dual Stripline
	<i>Rel.</i>	Ground_Plane
	<i>H Er</i>	FR-4
	<i>T</i>	Signals_Inner_2
	<i>C Er</i>	FR-4
	<i>T</i>	Signals_Inner_3
	<i>H Er</i>	FR-4
	<i>Rel.</i>	PWR_BTM_+5V

Variable	Value
Permittivity (Er)	4.6
Thickness of dielectric (H)	0,010"
Thickness of dielectric (C)	0,010"
Cu Thickness (T)	0,0007"
Trace width (w)	0,010"
Characteristic impedance (Zo)	49.4772 Ohm
Trace capacitance (Co)	6,9988 pf/inch
Propagation delay (Tpd)	2,1812 ns/ft
Inductance (Lo)	17,133 nH/inch

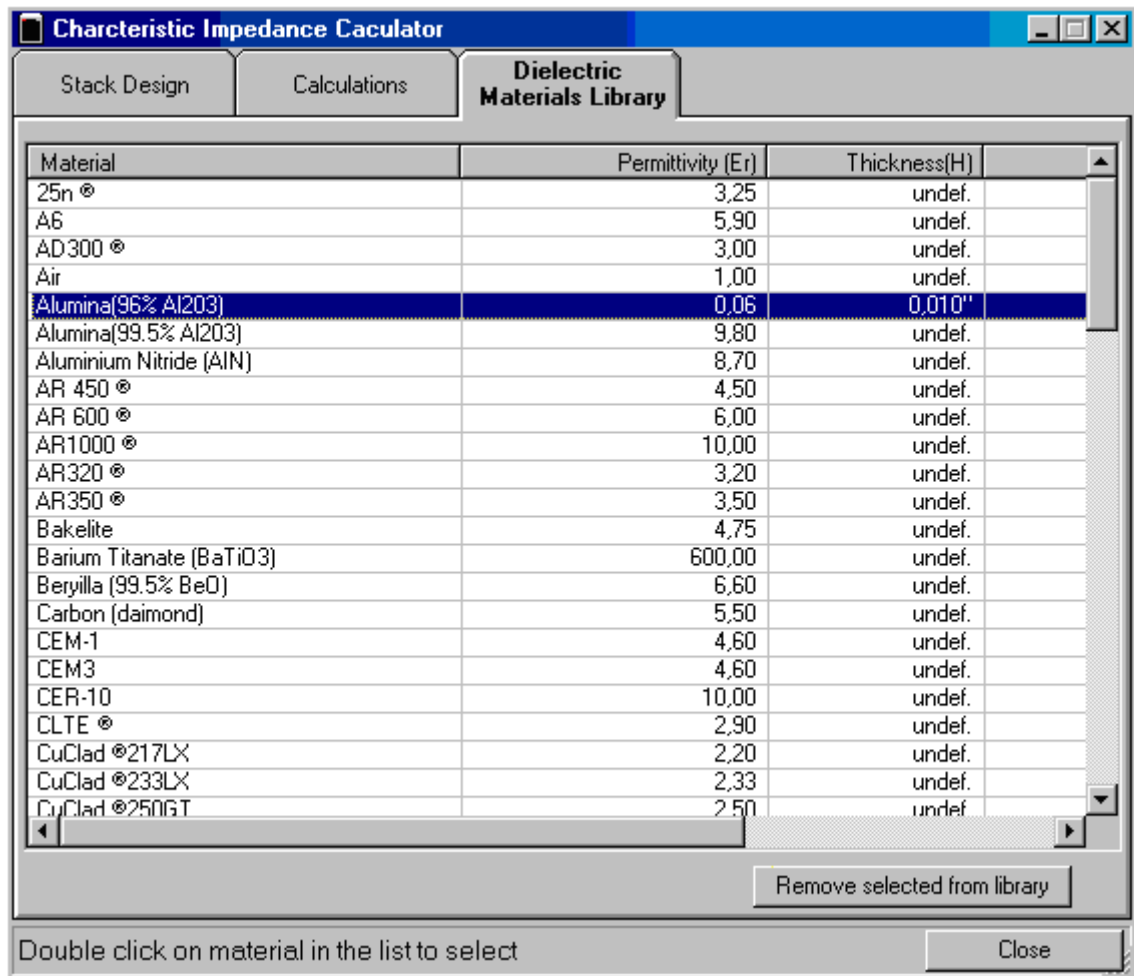
Calculate variable: [Click to select variable](#)

Output report to file

Close



Library of common dielectric materials is integrated with calculator. Entries in this library may be edited by the user and new materials added:

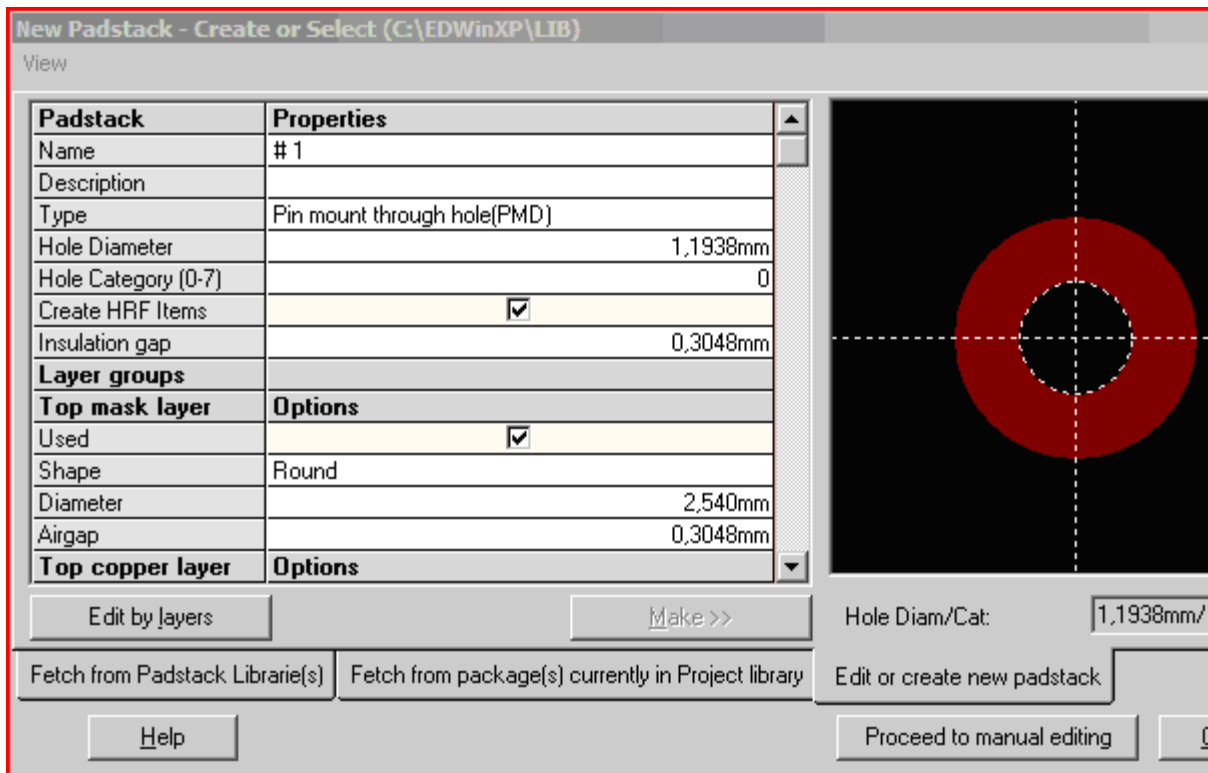


What's New in EDWin XP1.70 - Library Editor

Various improvements have been added to this application. Few "Dead end" dialogs have been replaced by dialogs pointing out to next possible operation, which in most cases is opening of Library Explorer for picking up elements for editing. Functionality has also been enhanced by adding several suggested features.

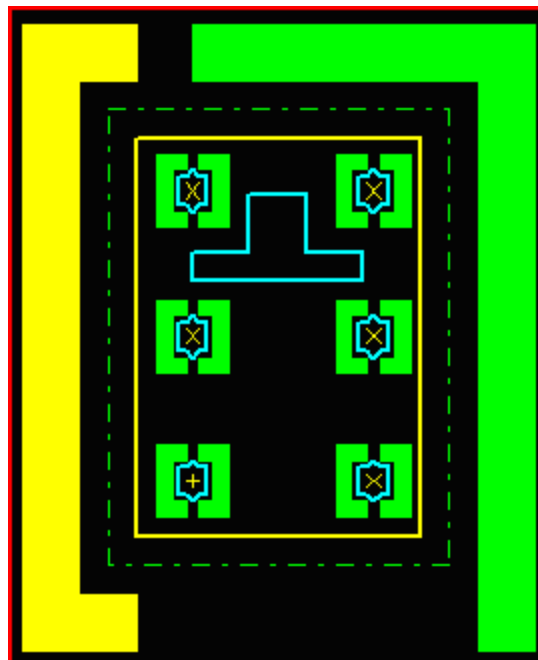
New dialog for pad stack design:

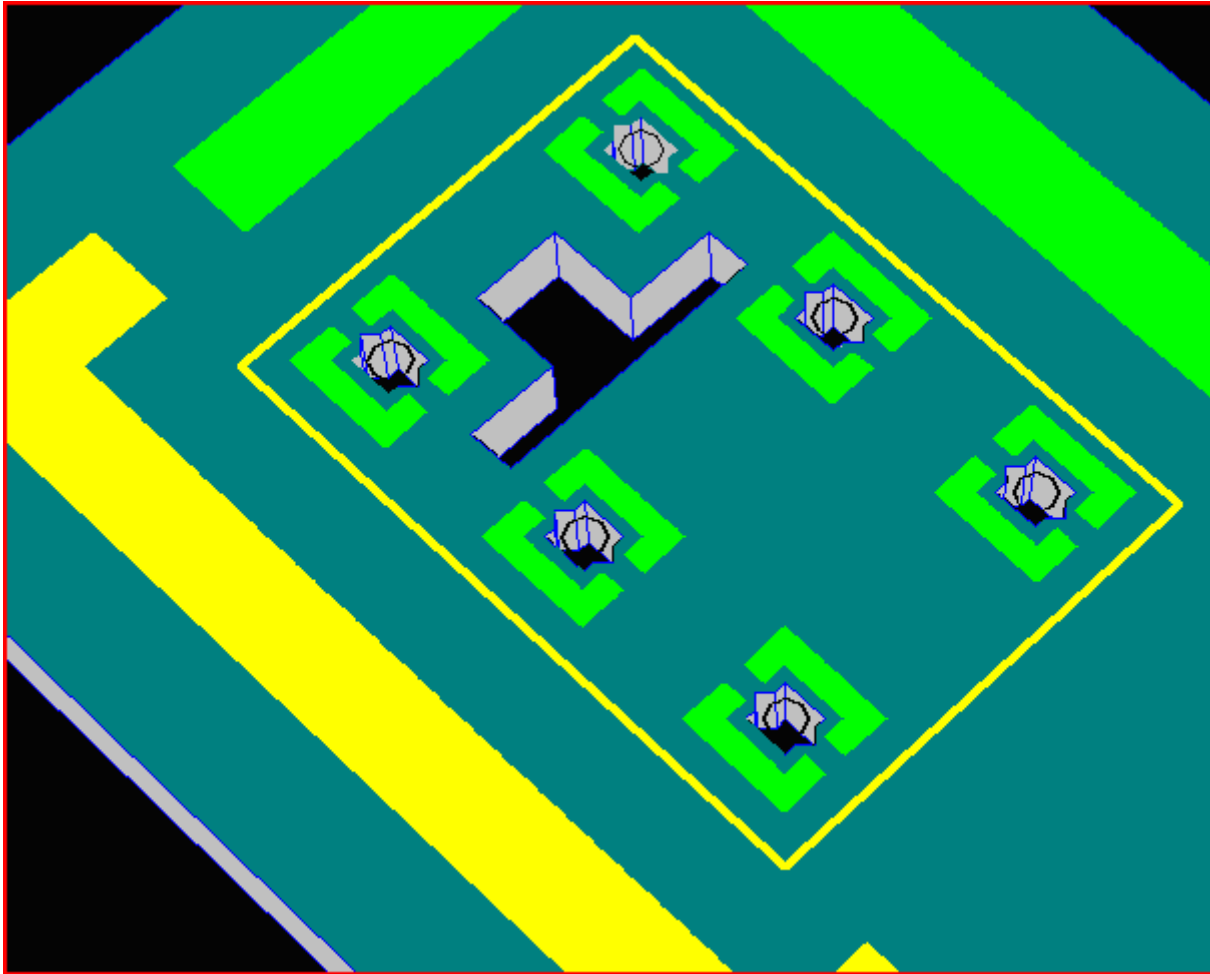
The dialog that open selections of pad stacks for editing (or inserting into packages) has been completely redesigned in order to make the whole procedure more straightforward and at the same time allow more flexibility. The user has now possibility to select and dimension one of supported standard shapes (round, square, rectangular, oval or rounded rectangle) for layer groups or individually for each layer. Pad stacks loaded from library may be modified using this dialog, eliminating in many case necessity to edit elements of pad stack manually.



Polygons in packages, symbols and pad stacks:

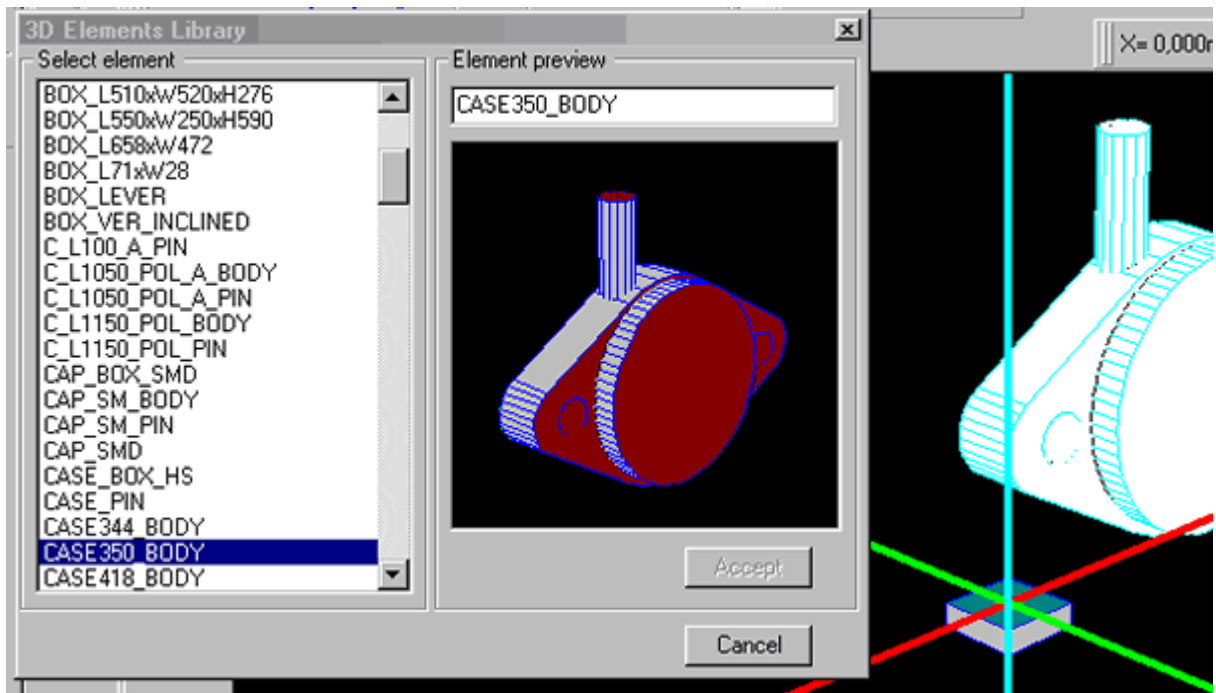
Some users expressed need to create "free-hand" shapes, especially in pad stacks. Whereas it was possible even before to create any copper/outline shape using basic graphic items like lines or rectangles, it could be laborious for shapes that are more complex. This problem has been addressed in 1.70 by introducing polygons as items in all graphical library elements. Polygons may be filled or of open outline type with specified line width. In packages and pad stacks, they represent copper (if not placed on top and bottom silkscreen layer). For these two kinds of library elements, the polygons may be also assigned special properties. In packages, they may be used to define boundaries of router keep-off zones, private for components using such package. Both in packages and pad stacks, polygons may be assigned property "slot". This allows for creating cutouts for each component on the board with reference to packages where slot were defined .





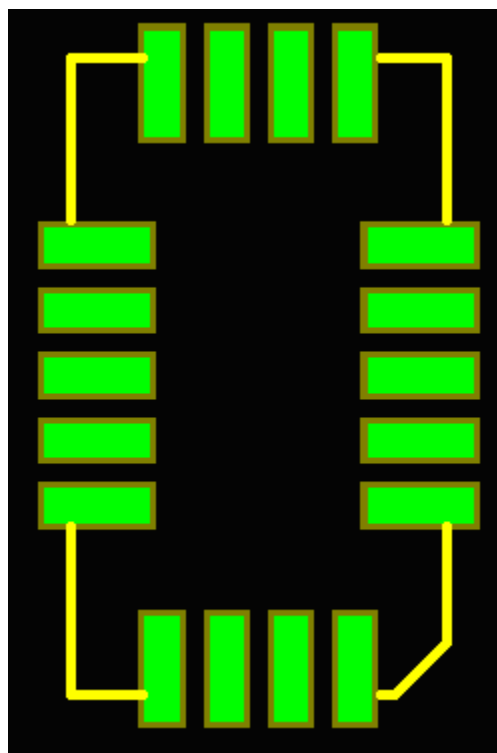
3D Elements Library:

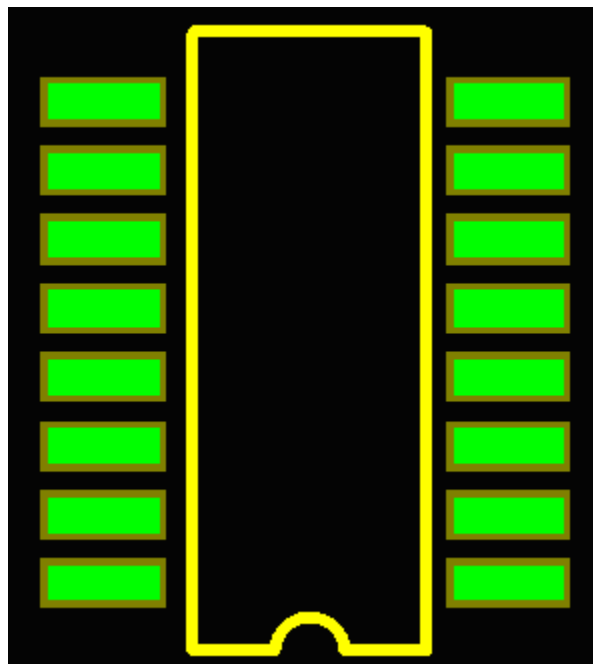
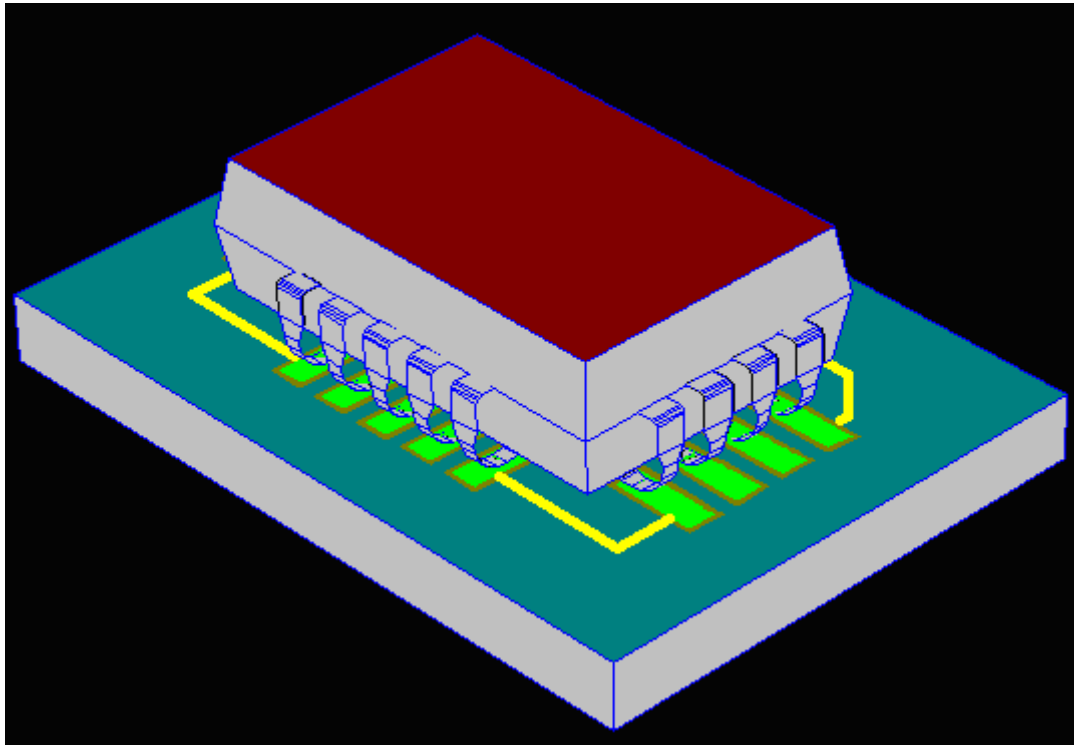
Editing 3D views of packages is rather laborious process. We have followed suggestion of one of the users and added a special purpose library consisting of more than 150 properly dimensioned 3D elements that may be used as building blocks for 3D editor. Elements include pins, bodies and other details that we normally use while creating package 3D views. At any time, the library may be opened and selected element inserted into currently edited package. Inserted elements may be subsequently relocated to their desired location.

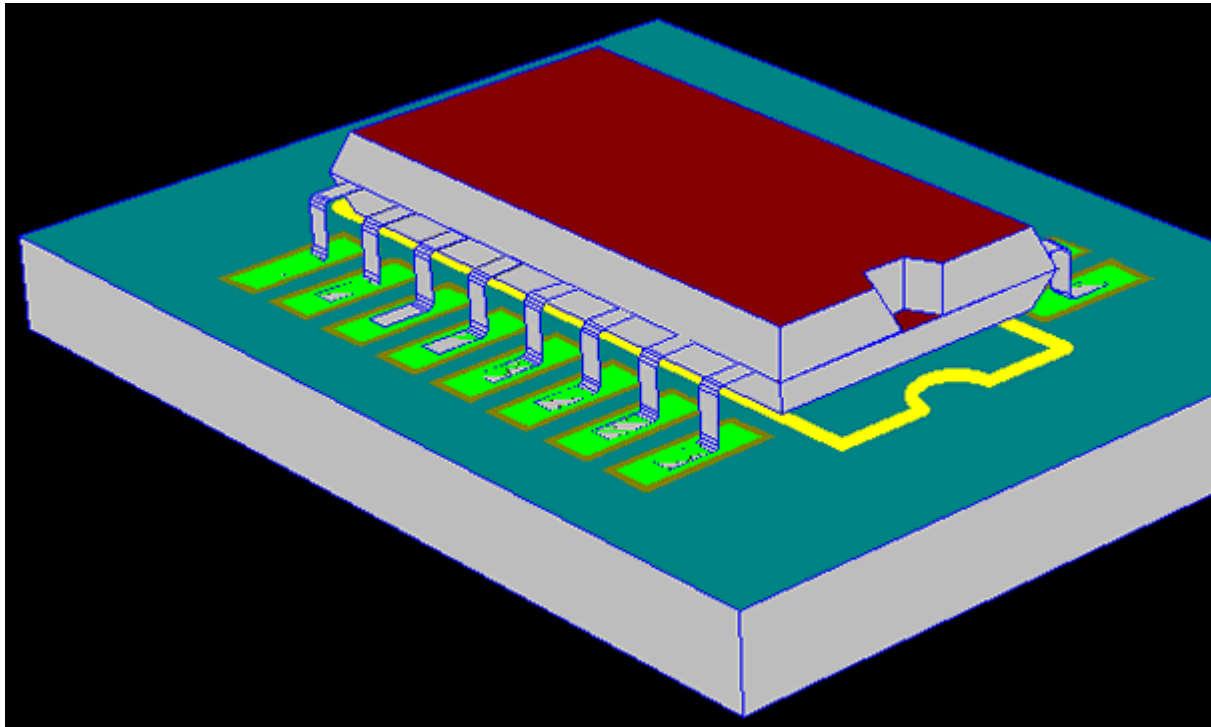


New package types in Package Wizard:

Package Creation Wizard has been enhanced with two new types - PLCC and SOIC

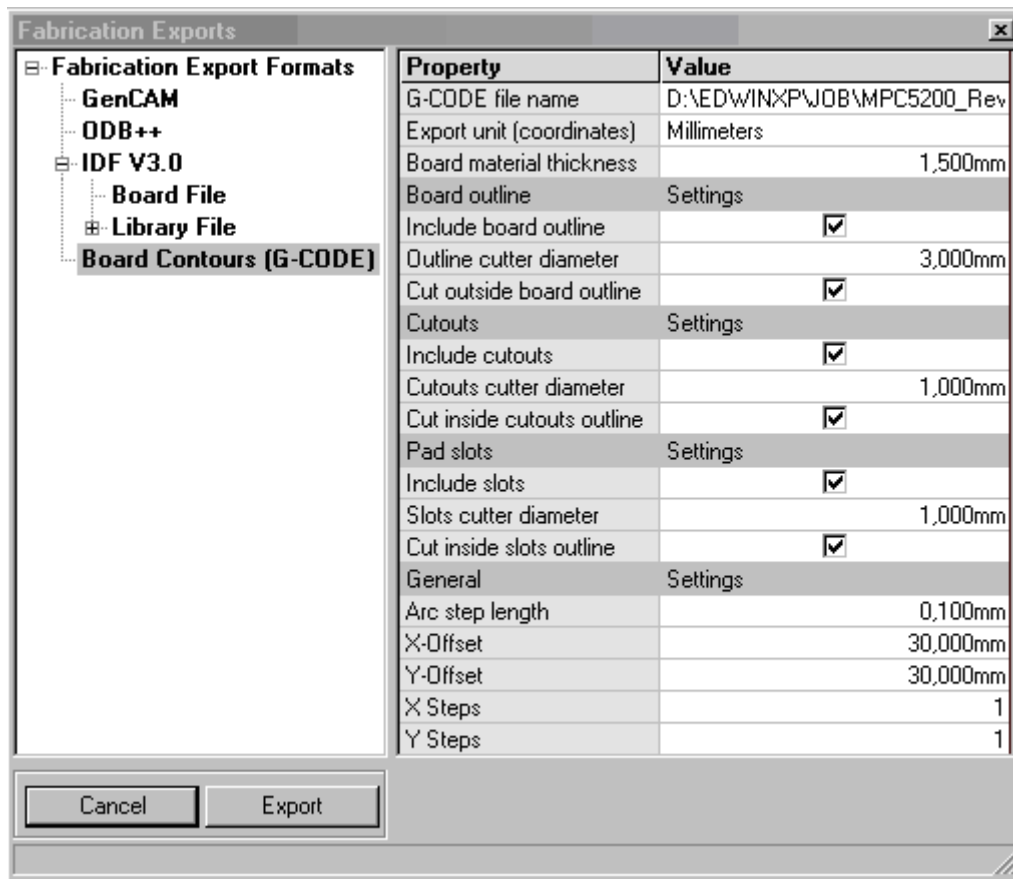






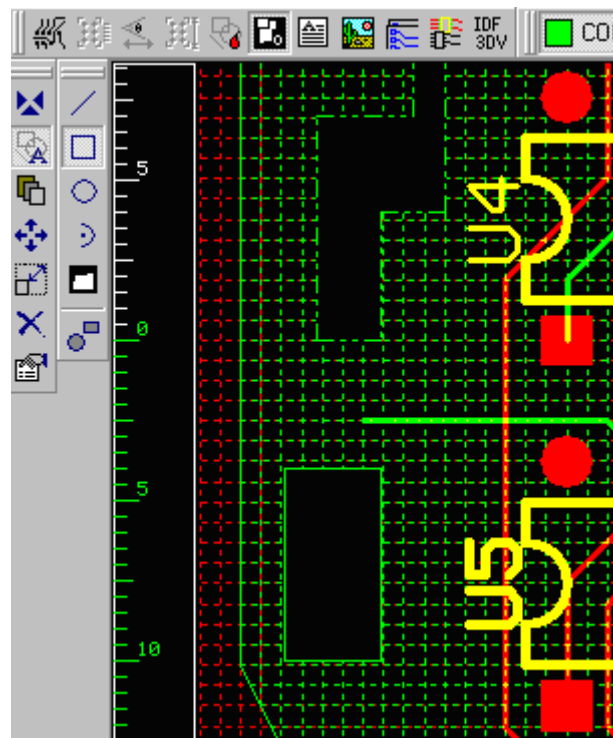
What's New in EDWin XP1.70 - Fabrication Manager

Changes in G-code export : Introducing slots in packages and pad stack, as well as tapered traces required several changes in Fabrication Manager, Gerber output. The slots are represented on artwork images as board outlines (exactly in the same way as cutouts). Since slots and cutouts are usually done using milling machines, G-Code export has been enhanced to include also those. Cutting slots (because of their small size) requires in most case usage of other tool that for cutting external outline of the board. It is now possible to assign tool sizes individually for board outline, cutouts and slots. This information is needed by the program to calculate trajectory of the toolpaths



Separate toolbar for Copper Relief editing :

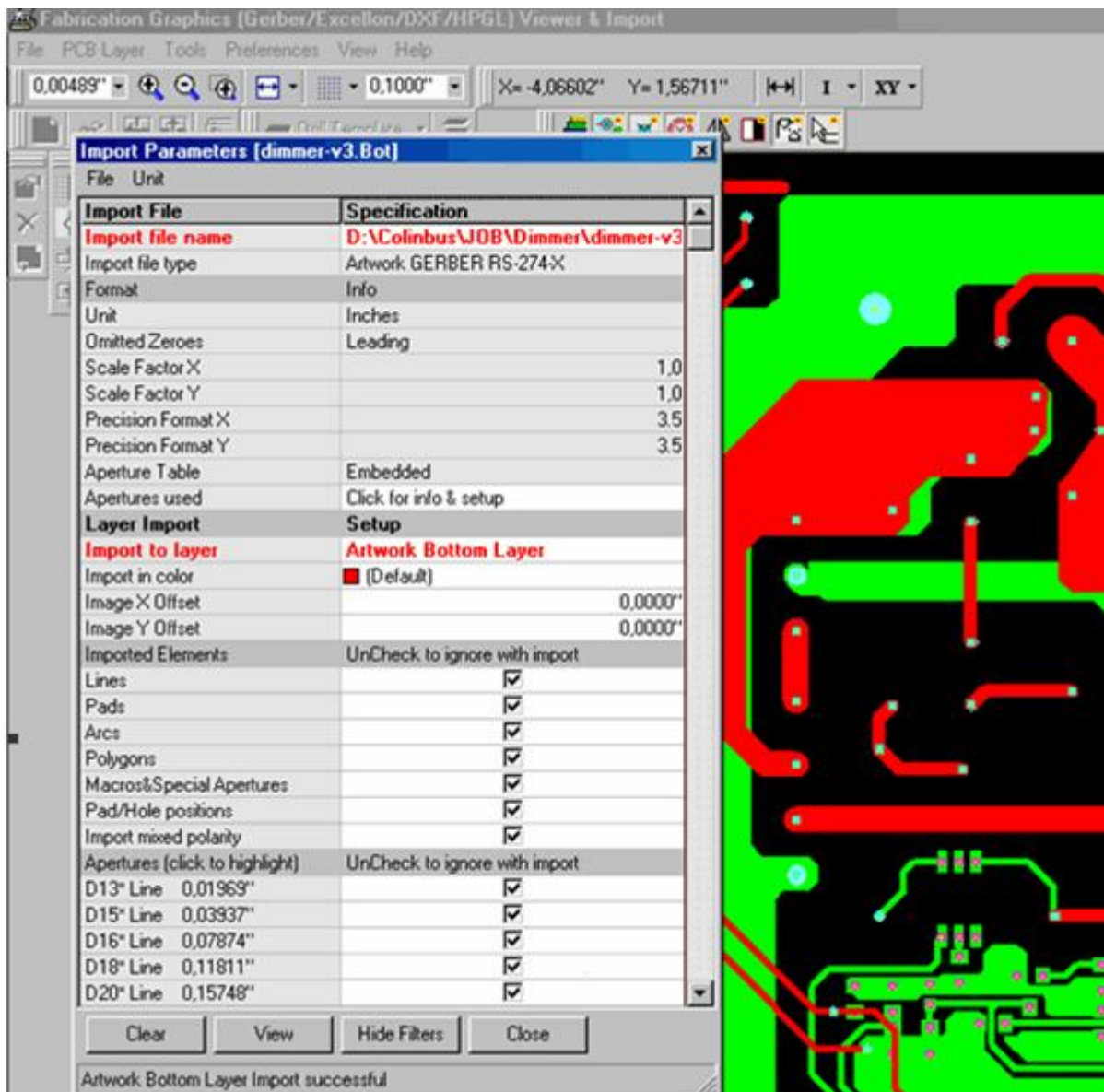
Possibility to focus display on entered X, Y-coordinates has been added to redraw modes in all editors.



Gerber viewer replaced:

Gerber viewer has been removed from Fabrication Manager and replaced by a new application called Fabrication Graphics (Gerber/Excellon/DXF/HPGL) Viewer & Import). New viewer may be invoked

from Fabrication Manager menu or directly from Project Explorer. It is now more convenient to examine GERBER artwork images in separate window when comparing with artwork images displayed by Fabrication Manager. Repertoire of supported formats has been completed by Excellon drill format and by HPGL. This last format together with AutoCAD's DXF is intended for importing board outlines. It is no more needed to preprocess any files. If a file selected for import is in any of supported formats, it will be automatically detected. Nevertheless, it is necessary to enter formatting parameters for files in obsolete formats like Gerber files in RS-274-D and Excellon One. Special function incorporated in the new viewer converts imported data to import categories that may be edited in Fabrication Manager prior to reconstruction of projects from graphics. The viewer has the capability for automatic distribution of imported data to most suitable category.



What is new in EDWinXP Version 1.61?

Version Controller

Project version control enables storing of different versions of a project in the same disk file. Current version may be saved at any time and all saved versions become part of the same project database. Any saved version may be restored immediately and set as current. Since all recorded versions are included in the same database and are loaded from and stored in a single

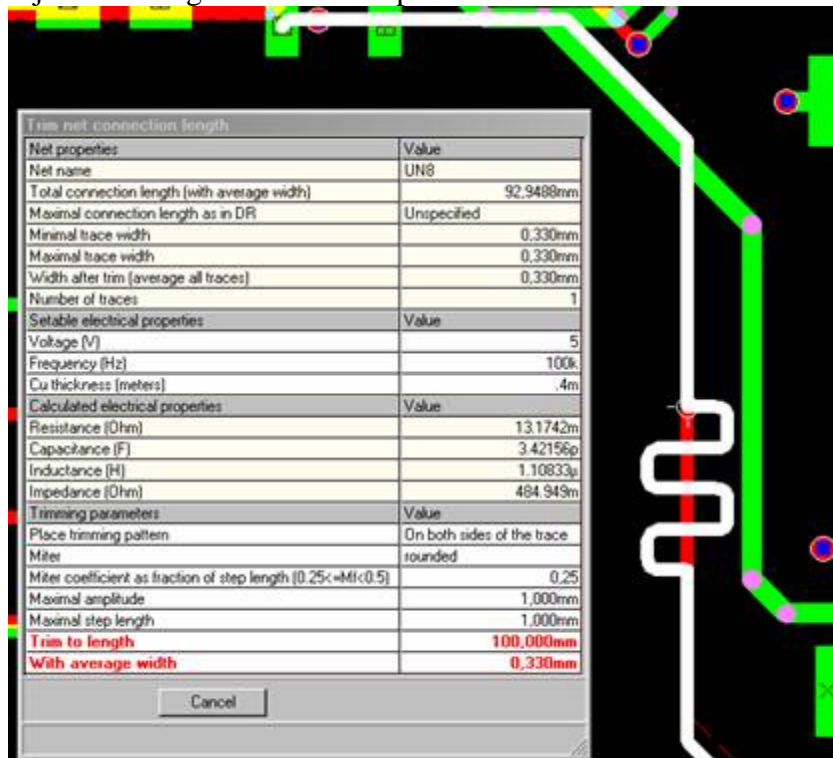
common disk file, there is no need to keep track of different version files and worrying about backups. It would be enough to back up only one file containing all recorded versions. It also allows to reconstruct single project database with several versions that were stored as separate database files (.epb) in previous versions of EDWinXP. There are provisions to view general and statistics informations and also to compare selected version with the active version. The new structure of database makes it incompatible with previous version of EDWinXP. Older project are fully upward compatible, can be loaded and will be automatically converted to the new format. There is also possibility to save selected project versions in a separate file in the format accepted by older releases of EDWinXP.

Note :This feature is available only for EDWinXP Commercial.

What is new in EDWinXP Version 1.60?

For this year's release, we have concentrated our efforts on implementing as many as possible suggestions collected from our users. Due to the character of these suggestions most new features have been added to Layout Editor, Fabrication Manager and Library Editor.

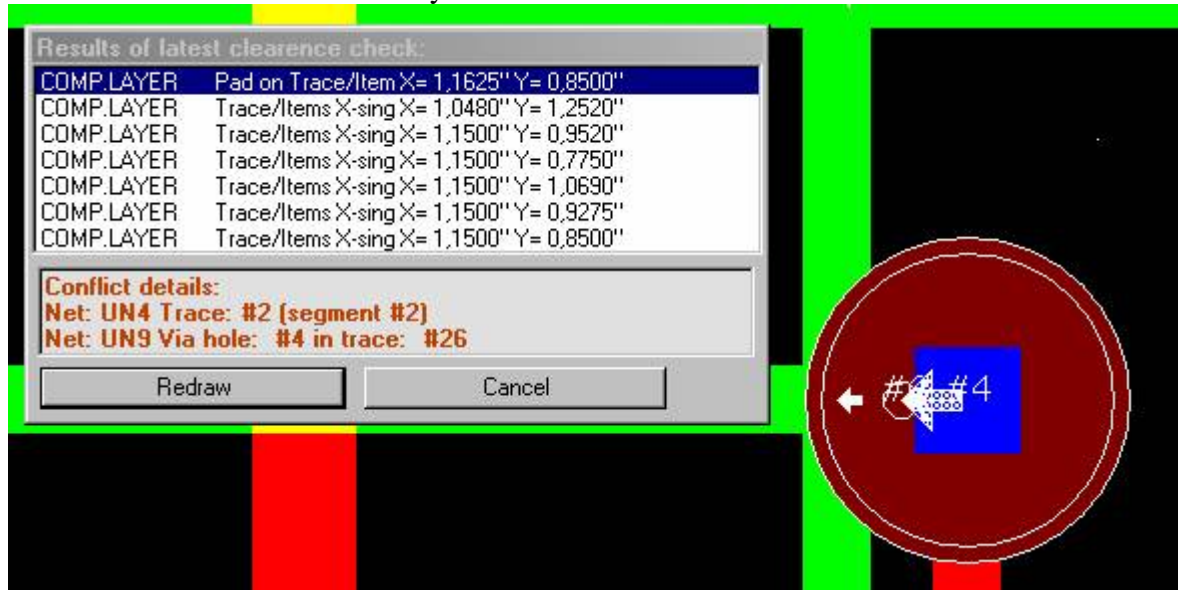
Trace Length and Width Trimming This feature allows inserting pattern of segments into selected trace in order to obtain exact specified length. The shape of the pattern, its amplitude and step length may be set as parameters for calculation of necessary number of steps. All user has to do is to select the suitable point in the trace where the pattern should be inserted. This is done interactively - the pattern (generated according to currently set parameters) is visible and follows cursor while it is moved along the trace. Parameters may be adjusted during this time until permanent insertion is confirmed by the mouse click.



Trimming function works in three modes: trimming single trace to specified length, trimming two traces to the length of longer one and trimming net connection to specified length. In the latter mode, it is possible to see how changing of length and average trace width affects net's electrical properties (resistance, capacitance, inductance and impedance) As further requested improvement, the current trace length is dynamically calculated while trace is manually routed or re-routed.

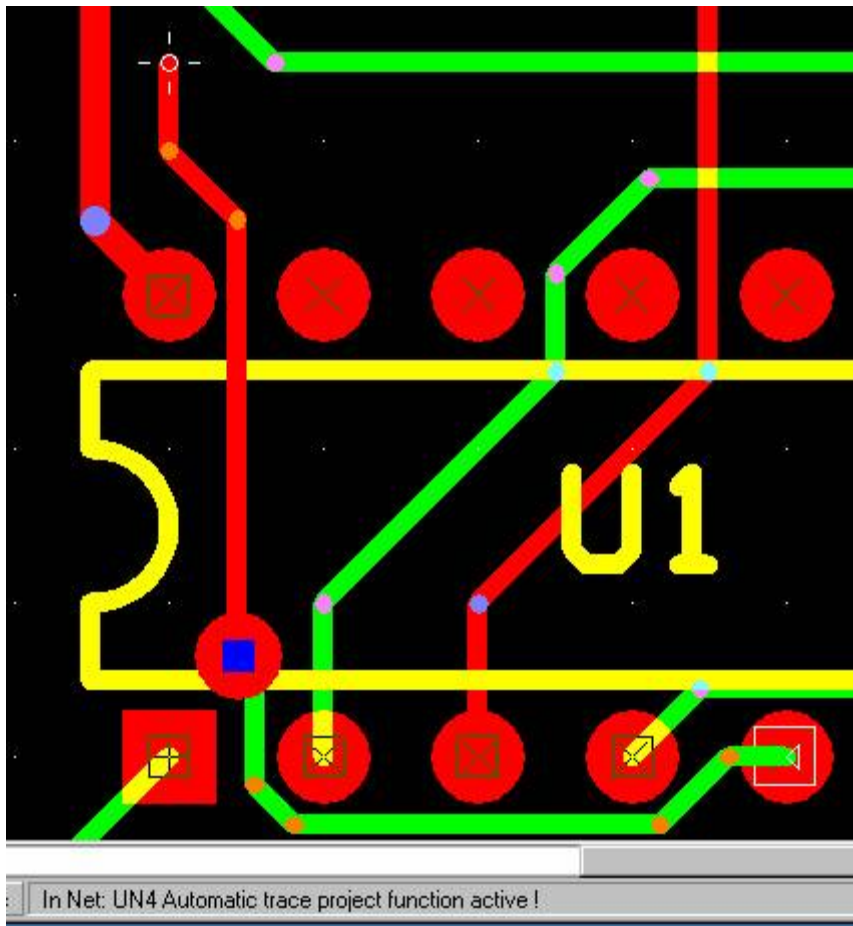
Automatic correction of selected clearance errors Reporting of clearance errors have been improved by providing additional details of detected conflicts. The dialog presenting locations of conflicts is always visible (modal) while navigating from error to

error. Focused errors are distinctly marked for exact identification.



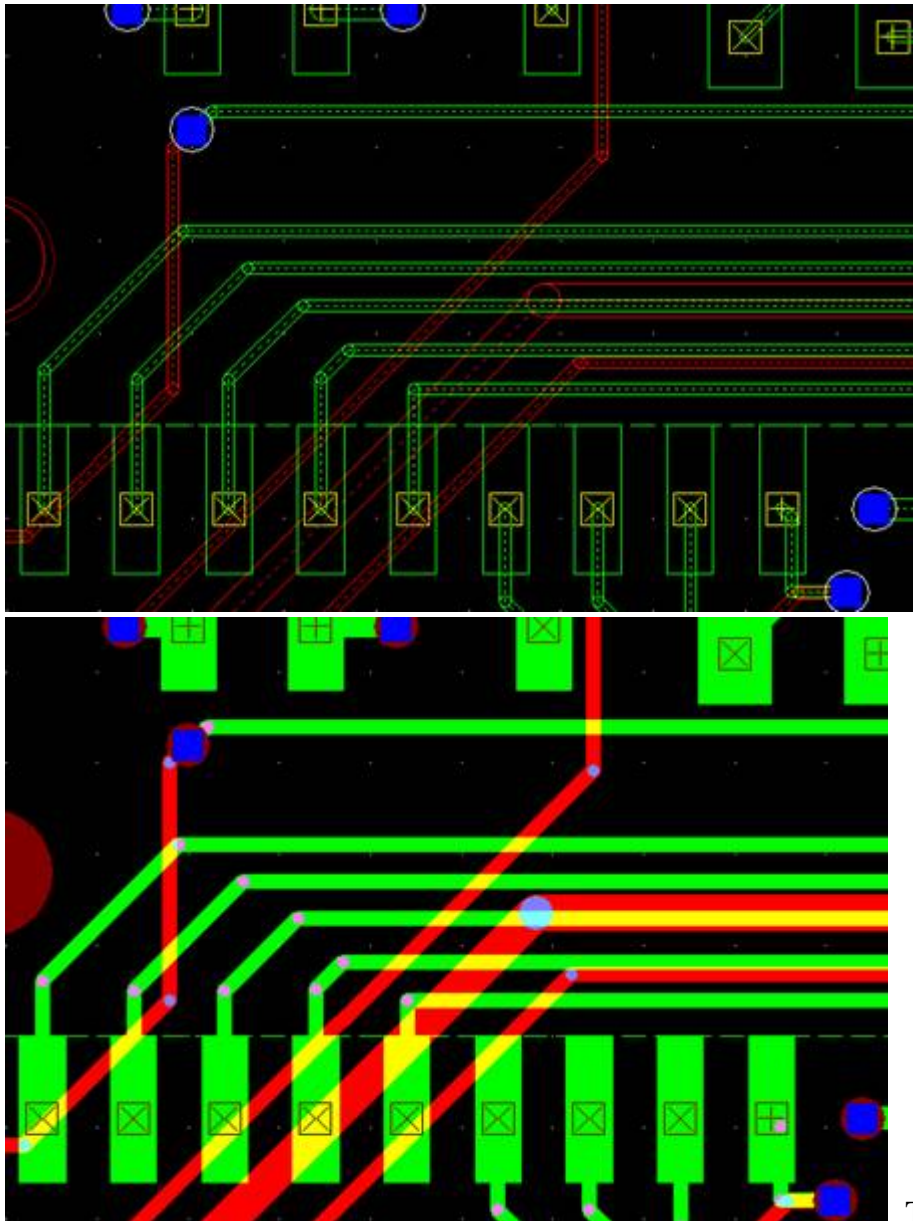
Another new feature is automatic correction of selected clearance error. This function works in two modes. Error to correct may be selected by pointing corresponding marker on the screen. The program is now able to recognize exactly which traces are in conflict. The one that creates most conflicts is automatically rerouted. In other mode, the user may select any of conflicting traces and order its automatic rerouting. **Automatic clearance correction after routing and rerouting.** On-line clearance error check introduced in previous version reported detected errors while a trace was routed or re-routed and after these operations were completed. In version 1.60, the on-line clearance check feature has been strongly enhanced by automatic correction of all clearance errors caused by the last route or reroute operation. This function has several options. It may be specified that correction should be executed always when error are detected without asking. Alternatively, information that errors have been detected is displayed awaiting confirmation for executing correction. It is also possible to order that correction should apply to the last routed/rerouted trace or that this trace must be left unchanged and only other conflicting traces should be automatically rerouted. **Automatic "trace project" feature** Pressing key combination, **Shift A** when a trace is manually routed or rerouted activates and deactivates automatic "trace project" function. Following happens, depending on currently executed operation:

- When a new trace is created and the function is ON, the program automatically routes clearance error free connection from the last inserted point to current cursor position. Cursor movement changes this so-called "trace project" to reroute dynamically depending on obstacles encountered on the way. Mouse click confirms that trace project to this point is accepted and subsequent trace project starts to be routed from this point. Even if the route suggested by trace project is not accepted, the feature may be used to seek best way for manual routing. It is possible to alternate (by **Shift A**) between the modes and route some parts of the trace manually and some parts automatically.

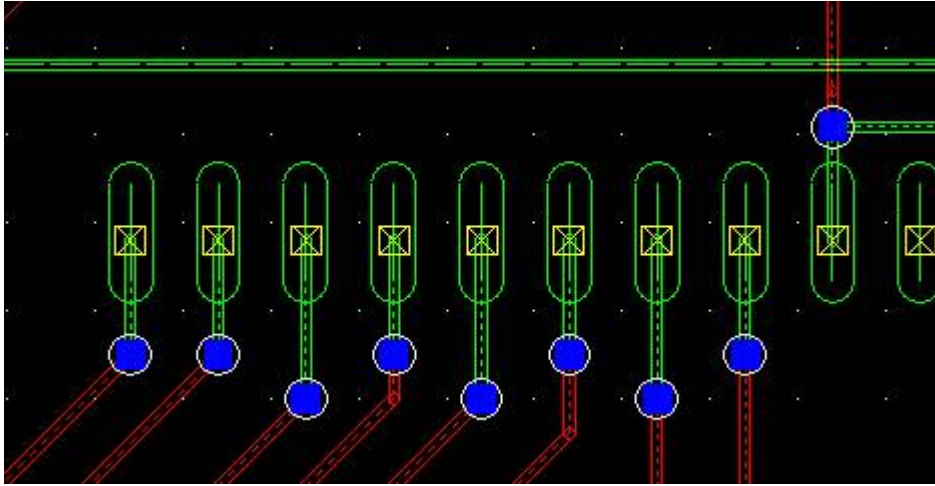


- When a trace point or segment is relocated, and the automatic trace project function is ON, the program reroutes preceding and following segments of the trace, starting in both directions from current cursor position. Using option "rip-up before reroute" allows in this case rerouting of entire connection between two nodes.

Project trace is routed according to design rules and auto-routing parameters currently set for the net. **Improvements in layout visualization** Often requested, so-called "XOREd" display of traces has been implemented in 1.60 release. In previous versions, traces on one layer were invisible if overlapped by later created traces on other layers. Even "stacked layers" option did not help much because the problem was reversed. In the new version, the display color changes in places where traces on different layers crisscross or overlap, creating effect of "transparency". There is also a new mode for displaying connections - Trace Frames mode. This mode when switched ON produces two effects depending on whether the layout is displayed in True Size or Centerline mode. Screen shots below present same area of the board displayed respectively in Centerline and True size modes and with Trace Frames mode set to ON. The traces are visualized by their contours allowing accessing their actual width and simultaneously to "see through" traces on all layers.

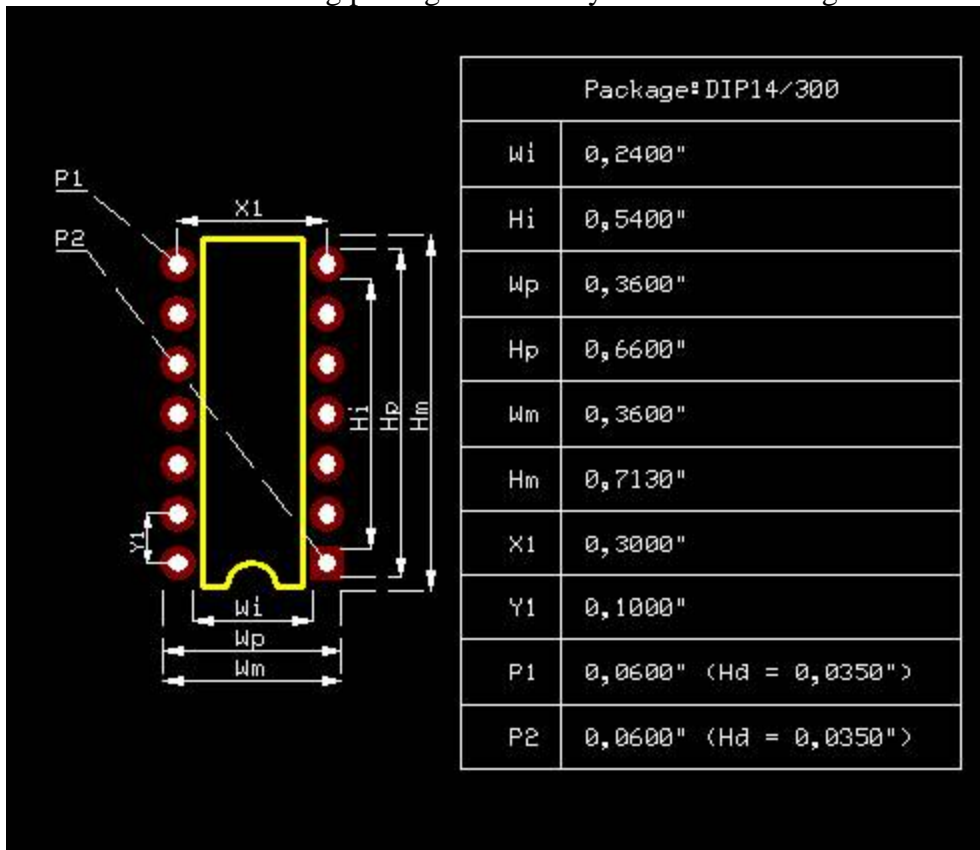


The transparency due to "XORed" trace display is clearly visible on the picture above showing True Size mode view. Trace Frames mode produces in this case small reddish circles representing position of bending points. This feature helps in detecting redundant bending points (inserted often by careless manual routing) that create unnecessary collinear trace segments. According to the same rule, oval pads created from lines of certain length and with are presented in contoured form that allows seeing their real size outlines in Centerline view mode with Pad Frames ON.



(By the way, also on users' request, Padstack Creation Wizard has been equipped with possibility to create rectangular SMD pads with rounded corners). Other issue connected to padstacks that has been solved in this version is the possibility to create SMD pads on top and bottom layers. Check for connectivity in Layout Editor that did not allow connection of trace to bottom placed pad in a component placed on top layer has been accordingly changed. This especially makes creating of packages representing finger connectors easier and more straightforward.

Auto dimensioning of packages and padstacks Users who produce boards on order often need to document library elements created for each design, even in printed form. For this purpose, dimensioning of packages and padstacks has been implanted in version 1.60. Tables with dimensioning data in following form are created fully automatically after switching to this mode while editing packages in Library Editor or viewing them in Package



Viewer:

Shortcut to copper check added to flood test in Layout Editor Checking for short cuts to copper pour areas were in previous version cumbersome because it required

starting Fabrication Manager and use of function provided for editing artworks. Now, the flood test for copper pour connectivity that has been implemented in previous version has been enhanced to include also shortcut check. In this manner, all layout design testing functions are finally grouped in one application. **More padstacks for via holes** On users' request, number of available padstacks for via holes (previously 7) has been increased to 16. To facilitate differentiation among various padstacks, it is now possible to add labels to each of them for individual recognition. It is even possible to highlight vias using given type of padstack. **New features in Fabrication Manager** Undo/Redo was missing in this module, which is especially needed when reconstructing projects from graphic imports. This has been remedied in new version. Other problem encountered in this field was lack of simple means for aligning images imported to categories. This issue has been solved by adding alignment function. New fabrication export has been implemented, this time for exporting CNC data in G-CODE format containing generic machining program for cutting board outline contours and internal cutouts. Toolpath for cutting are calculated allowing for specified cutter diameter (cutting outside outer contour and cutting inside internal outlines). **Mouse wheel** Support for mouse wheel has been fully implemented in version 1.60. The wheel is used for zooming graphic display in and out with simultaneous panning to point shown by the cursor. Mouse wheel may be also used to scrolling up and down the tables (grid control) that are displayed in pop up dialogs **New List of Material Editor** Previous version of this program was difficult to use. This module has been replaced by completely rewritten new version that on one hand allows creating simple lists much easier and on the other allows using advanced feature of External Info Database in more straightforward, intuitive way. Additionally, output filters have been introduced enabling to generate variants of BOMs from the same project database. **Vista compatible help system** All help files have been converted and re-edited for compatibility with Microsoft Vista operating system. **Project version** EDWinXP 1.60 includes project version control that enables storing of different version of a project in the same disk file. Current version may be saved at any time and all saved version become part of the same project database. Any saved version may be restored immediately and set as current. Since all recorded versions are included in the same database and are loaded from and stored in a single common disk file, there is no need to keep track of different version files and worrying about backups. It would be enough to back up only one file containing all recorded versions. The new structure of database makes it incompatible with previous version of EDWinXP. Older project are fully upward compatible, can be loaded and will be automatically converted to the new format. There is also possibility to save selected project versions in a separate file in the format accepted by older releases of EDWinXP. **New microcontroller kit and simulation models** We are releasing also new models created in MMI technology for: Line 5 x 8 dots LCD display full version HD44780U LCD display driver full version full version Line 5 x 8 dots LCD display Line 5 x 10 dots LCD display Voltmeter (instrumental) GLED OrLED As well as standard digital models: 74F579-8-bit bidirectional binary counter (3-State) 74F597-8-bit shift register with input flip-flops **Many small improvements** Many requested small improvements have been added to the system and not all of them are clearly visible. Just to mention a few: **Ctrl** key doubles as * (asterisk) to initiate entering of shortcut commands. This has been added for improved ergonomics. Content of data created by List Generator program has been extended to include component values. Measurement function recognizes more object types (board outline) and displays not only distance but also delta X and delta Y between measured objects. Nodes in Net Property dialog (Schematics Editor) are displayed grouped by schematic pages where they are located. Pins numbers in Component Property (Layout Editor) dialog are displayed with corresponding schematic entry names Refreshing of

elements in Project Library may be done selectively. Opening of padstack editor may be done directly from Layout Editor. [Tillbaka till EDWin sidan](#)

EDWinXP Version 1.50

1.

ODB++ Export

Gerber and NC Drill data is capable to provide the information to fabricate the PCB. But the increased complexity of the PCB's, combined with the need for faster design turn-around has resulted in the emergence of new CAD/CAM data formats. The most popular of these is ODB++ captures all PCB fabrication and Assembly data in a single, unified database.

EDWinXP project is first exported in ODB++ Gateway format.

Subsequently, a third party converter called from EDWinXP in order to translate ODB++ Gateway format into full Job description in ODB++ format.

2.

ODB++ Import

Import projects of CAD packages which supports ODB++ formats to EDWinXP. Import of each ODB++ job step consists of three automatically following phases.

1. The program reads EDA part (packages, components and netlist).
2. Geometrical features (positive polarity only) of board layers are imported.
3. The reconstruction of read data into editable EDWinXP database objects (This stage is optional).

3.

Filter Designer

Filter Designer is to design different types of filters by entering specifications in the Schematic Editor. This will generate Filter circuits in the schematic editor, which can be used as part of other circuits. Different filters included are

1. Chebyshev
2. Butterworth
3. Bessel
4. Elliptic (Cauer)
5. Ideal

4.

Add Solder paste/Glue mask item to padstack

This new facility available with the new version of EDWinXP, automatically updates Padstacks for SMD pads with **Solder Paste / Glue Mask items** on the layer selected by the user. The user may select rectangular, square, oval or round shaped Solder Paste / Glue Mask item. The new

feature presents list of layer pairs that are currently unoccupied in a PCB and one may be selected as Solder Paste / Glue Mask layer. The user can express in percent or as a fixed value for the dimensions of Solder Paste / Glue Mask items for the layer that has been selected and will be removed and replaced by newly generated shape.

5.

Copper pour connectivity test

Copper pour connectivity test have been added in the PCB Layout Editor. Similar test was already included in Fabrication Manager. The advantage of this test in Layout Editor is that the connectivity may be checked while the board layout is designed. In both modules, the test may be now performed in selectable accuracy of 0.100, 0.050 and 0.025 mm. The time needed to execute the connectivity test has very significantly reduced.

6.

New Features in PCB Layout

1. View Holes
2. Ratsnest for unconnected node only
3. Online Trace clearance check
4. Increased number of tools in automatic routing
5. Re-routing the traces in two modes
6. Improved visualization in node marker and pin entry marker size

7.

New Features in Fabrication Manager

1. Improved Gerber Viewer Setup
2. Square Holes in Gerber Artwork
3. Improved Reconstruction of projects
4. Enhanced Copper Removal

8.

New libraries and Simulation models

75 new libraries are included in EDWinXP 1.50.

The new models available in

Mixed mode Simulation model: 11 new models added including Stepper motor , Potentiometer, Alpha numeric display etc.....

EDSpice Simulaton model : 16 new models , 5 circuit files and 3 sub-circuits.

10 Sample projects with new EDSpice subcircuits

[Tillbaka till EDWin sidan](#)

EDWinXP Version 1.40

What's new in this version? Many new features have been added to the system since release of EDWinXP Version 1.30. Certain number was already made available

to current users of version 1.30 through Live Update. Nevertheless, some improvements were implemented on individual users request and never distributed generally. All these changes are now incorporated in version 1.40 as standard features. Apart from that, this version includes new functions that were never available in EDWinXP before. **Schematics Editor and Simulators**

- **Block Diagram Elements**

This feature allows for simplified creation of block diagrams of hierarchical circuits. There is no longer need to create block diagram elements using Library Editor since part descriptions and symbols are automatically created according to user's specification. Nevertheless, parts and symbols created for block diagram elements may be edited like any other library element and stored in the disk libraries for farther use.

- **Component Specific MM Simulator Models**

Mixed Mode simulation models may be assigned individually to components, hence overriding current model assignment to symbols. Component specific simulation models may be assigned to block diagram elements.

- **Truth Table to diagram converter**

Logic function defined in form of truth tables may be converted to equivalent schematic diagram that may be later attached to currently edited page, form a new page in edited circuit or be attached as new circuit in the project.

- **VHDL Code to diagram converter**

Similar feature as above but the logic function of a diagram is specified by editing and compiling VHDL code.

- **Direct assignment of logic function to schematic components**

Logic function of selected schematic component may be specified either through truth table or VHDL code and attached in form of hierarchical sub-circuit or automatically generated simulation model. Generation of both MM Simulator and EDSPICE code models is supported.

- **Instant probes**

Instrument that allows for instant time domain simulation and waveform presentation on selected points in the circuit.

- **8051 Microcontroller Kit**

The kit contains new simulation model of microcontrollers of 8051 family and application examples. The 8051 model uses MMI technology that enables edition and compilation of programs in C-language and assembler, debugging the code and

simulation together with whole circuit. Attached simulation examples help in evaluating the kit and learning how to use the model for the development of microcontroller programs. The kit contains also series of so called instrumental model for generating parallel and serial binary data patterns and asynchronous hardware interrupts. Usage of 8051 model in user's designs requires separate license.

- **Vertically or horizontally oriented net/bus page link notes**

Depending on user's preference, net/bus page link notes may be generated either as vertical or horizontal bar. Vertical bar was the only option in previous versions.

Fabrication Manager

- **Improved multilayer copper pour connectivity check with 3D presentation**

Previously implemented copper pour connectivity check has been enhanced for simultaneous testing of all artwork layers where connections for selected net are present. User may examine location of detected unconnected or isolated pads and isolated via holes with help of two or three dimensional presentation.

- **Polygonal copper relieve**

Definition of areas on the artwork where copper should be removed from copper poured Gnd/Power planes was previously done through placing items like rectangles and circles. In present version relieve areas may be defined by polygons. A feature useful for removing of isolated islands of copper that usually have irregular shapes.

- **3D export in IDF format**

Feature allowing for exporting 3D view of the PCB in IDF Ver. 3 format

- **3D IDF file viewer**

Three-dimensional presentation of IDF Ver 3 format files.

PCB Layout Editor

- **Multilayer copper pour connectivity check with 3D presentation included**

Copper pour connectivity check, working in similar way as in Fabrication Manager, has been added to PCB Layout Editor. 3D presentation may be used to visualize detected errors on all layers where tested net connections are located.

- **Improved presentation of copper pours**

On request, coppers pour areas may be presented filled by meshed pattern for better visualization of boundaries on densely packed PCB layouts.

3D Graphics

- **User definable true colors**

Apart from 32 standard colors, the user may define custom palette of 224 colors and assign them to objects in three-dimensional visualization.

- **Improved scrolling and navigating**

Current scroll position is retained when switching between 2D and 3D presentation. This is useful for examining results of connectivity check where alternating views without losing focus on the object is often required. Rotation of 3D view is executed around currently focused location rather than around coordinate system origin.

- **Semi-transparent view of copper pour areas and layout components**

An extremely useful feature for 3D visualization of multilayered PCB designs.

General

- **New netlist export format (RINF Netlist) 130 new parts in library**
- **14 new models for Mixed Mode Simulator**

[Tillbaka till EDWin sidan](#)